

ABSTRACT

Design, Simulation, Construction, and Measurement Testing of Fast-Reconfigurable Radio Frequency Switched-Stub Matching Networks

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Today's world is increasingly dependent on wireless communications, and fifth generation (5G) cellular technologies have recently entered the picture. Part of their designated spectrum overlaps with that of S-band radar systems. In order to effectively share the spectrum, the high-power radar systems must be able to transition to alternate operating frequencies in real time. To do this without sacrificing transmit range requires reconfigurable matching networks placed in between the power amplifiers and phased-array antenna elements in the radar transmitters which must be able to meet the power and speed requirements of the system. Historically, tuners have struggled to meet both requirements simultaneously. This thesis presents a simulated design, an algorithm to optimize reconfigure the circuit as operating conditions change, a low-power prototype switched-stub reconfigurable matching network, and a prototype taking advantage of custom semiconductor plasma technology with the purpose of progressing towards a solution that meets the radar system requirements.

Design, Simulation, Construction, and Measurement Testing of Fast-Reconfigurable Radio
Frequency Switched-Stub Matching Networks

by

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A Thesis

Approved by the Department of Electrical and Computer Engineering

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Submitted to the Graduate Faculty of
Baylor University in Partial Fulfillment of the
Requirements for the Degree
of
Master of Science in Electrical and Computer Engineering

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May 2021

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ACKNOWLEDGMENTS

I would like to thank Dr. Charles Baylis for both his guidance in my academic efforts as well as for taking the time each week to show genuine care for our group at Bible studies. I would also like to thank Dr. Robert Marks for his contributions and unreplaceable perspectives. Additionally, I would like to thank all of my fellow student researchers, current and former, who have assisted with difficult project and have become friends as well – Jose Alcala-Medel, Pedro Rodriguez-Garcia, Austin Egbert, Angelique Dockendorf, Adam Goad, Justin Roessler, Gordon Ledford, Ellie Langley, Ben Atkins, and Connor Laktasic. Thank you to our sponsors at the Office of Naval Research for funding my project under Grant No. N00014-19-1-2549 and to our collaborators, especially those at Purdue University – Dr. Dimitrios Peroulis, Dr. Mohammah Abu-Khater, Alden Fisher, and Zach Vander Missen. I would also like to thank my professors who have pushed me to learn and grow, filling some of the knowledge gaps that brought me to graduate school in the first place. Thank you to Mrs. Michelle Aars and Mr. Robert Baish for behind the scenes work, making procurement for my design iterations much easier. I would like to thank my family for their encouragement and support throughout my entire life and education. Finally, thank you to roommates and friends who have made this demanding time a whole lot more enjoyable.

ATTRIBUTIONS

Some of the work described in this thesis was the product of a collaborative effort with the authors of [28, 29, 30].

For [28], I collaborated on the design of the radio-frequency (RFF) topology, designed the physical circuit board, and performed the bulk of the measurements. Dockendorf collaborated on the RF topology, performed an initial algorithm comparison, and assisted in measurement testing. Egbert originally designed the algorithm and assisted in implementation of the algorithm, including porting the algorithm to the software-defined radio platform. Herrera assisted in the RF topology design, provided feedback for the circuit board design, and assisted in the antenna matching measurements. Baylis and Marks oversaw the project and provided feedback and direction.

In [29], I adapted the algorithm from [28] to account for the starting points of previous operating conditions. Egbert assisted by adding features to the software-defined radio and LabVIEW FPGA measurement system including compatibility with MATLAB. Dockendorf's starting point lookup ideas from an older tuner were foundational to my adaptations to the algorithm for this tuner. Baylis and Marks again provided direction and feedback.

For [30], I designed the new circuit boards and performed the measurements. Roessler assisted in much of the data collection. Egbert provided feedback for the board designs and continued to improve the software-defined radio measurement platform and

MATLAB control. Fisher designed and provided the silicon chiplets, and his previous work was the basis for the selected switch design. He also provided feedback in the circuit board design. Baylis helped steer the project and provided feedback where applicable. Vander Missen provided suggestions for elements of the circuit board design. Abu Khater, Peroulis, and Marks also helped direct the efforts and provided feedback and suggestions where applicable.

CHAPTER ONE

Introduction

The National Broadcast Plan of 2010 dictates that 500 MHz of the frequency band between 225 MHz and 3.7 GHz must be repurposed for shared usage [1]. Although much work has been performed towards meeting the goals of the plan, success has not been achieved after the ten years allotted for the plan [41], necessitating the plan be revisited with new perspectives of the environment, as the infrastructure has changed significantly in the last decade. More recently, other programs have been developed; including America's Mid-Band Initiative Team (AMBIT), which says that radar systems must share a portion of the S-band from 3.45 to 3.7 GHz with fifth-generation (5G) cellular devices [2]. Instead of that portion of the band solely being allocated to radar systems, radar users are able to coexist, so long as they do not interfere, in accordance with the plans. This coexistence requires a variety of creative solutions, including spectral sensing abilities, advanced signal processing, and reconfigurable circuitry in the radar transmit chains.

This thesis describes the design of high-power, quickly tunable reconfigurable circuitry for the radar transmit chain. One could opt to implement a broadband solution instead of tunable narrowband hardware. However, Roessler shows that an amplifier with a narrowband, tunable load matching network can obtain higher gain over a range of frequencies than an amplifier design using the same transistor, but terminated using a broadband load matching network instead [3], a result supported by the Bode-Fano criterion [42]. Roessler proceeds to show that up to a 16.9 percent improvement in radar

detection range can be achieved in his simulation study [3]. In this thesis, a circuit design is presented that can be reconfigured for optimal performance throughout the entire radar S-band from 2-4 GHz, while simultaneously solving issues presented by varying antenna impedance as the radar beam is steered spatially. Figure 1.1, below, shows a simple visual diagram of where the matching network would be placed in a transmit chain where it provides the desired reflection coefficients to both the power amplifier (PA) and the antenna element.

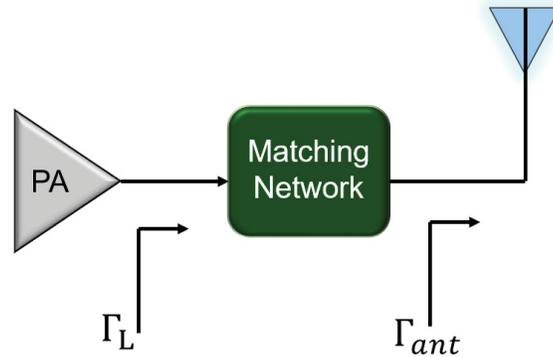


Figure 1.1. Visual indicating matching network placement between PA and antenna.

The ideal amplifier load matching network for a radar transmitter must handle the high powers necessary for an effective radar system, and should be able to be reconfigured quickly enough to allow uninterrupted use of the radar system. Radar transmitters must transmit with particularly high power levels due to the $1/R^4$ dependence of received power on distance R from the target, compared to a $1/R^2$ dependence for a communication system. Increasing the transmission power causes a larger amount of power to reach the target, increasing the power reflected by the target back toward the radar receiver. High-speed reconfiguration is desired to allow the radar

system to operate nearly continuously when changing operating frequency or array scan angle. Ideally, reconfiguration would be able to occur within the pulse repetition interval (PRI) of a radar system, allowing the radar to adjust its operations on a pulse-to-pulse basis. Semnani [46] describes the key issue at hand; high-power tuners are generally heavy and cannot reconfigure as quickly as desired, and fast electrically-tunable devices can only handle tens of watts or fewer. He provides a table comparing technologies, and his specific tuner can handle 50 dBm (100 W) with a single reconfiguration on the order of hundreds of milliseconds. High-power, electrically tunable switches with favorable radio-frequency (RF) characteristics can be the cornerstone of such a design.

Chapter Two provides further background information to provide a basis of understanding for the design and shine light on the state-of-the-art of related technologies and algorithms used to control them. Chapter Three details the RF topology design and simulation across the desired octave of frequency as well as the discrete algorithm development for optimizing such a device. Upon satisfactory results, Chapter Four shows how the RF topology was included in the design of a low-power prototype tuner, which intentionally used low-power switches and provided a foundation for test bench setup and algorithm testing and improvements. Lastly, Chapter Five describes the design, construction, and measurement of a tuner with high-power switches. Multiple design iterations to maximize the performance of the semiconductor plasma technology used for switching are described, including the introduction of microlenses. Chapter Six summarizes the results and maps a way forward for future high-power tuner designs.

CHAPTER TWO

Background

This chapter provides a brief description of the foundational ideas of impedance matching and microstrip matching networks that will help in understanding the remaining content of the thesis. Additionally, the state of the art of impedance tuner technology and algorithms are discussed, followed by an accounting of the contributions made by Baylor's teams and collaborators.

Impedance Matching Motivation

This thesis revolves around the design of a reconfigurable matching circuit, also known as a “tuner”. Figure 2.1 shows a simple block diagram containing the key elements in an RF power amplifier (PA). The pertinent items for discussion here are the PA, output matching network, and antenna. The output matching network is placed at the load side of the power amplifier, the matching network is designed to provide load reflection coefficient (Γ_L) values for desired performance in parameters such as output power, efficiency, noise, or linearity. The focus of this thesis is matching for optimal output power. When the operating frequency of a radar transmitter changes, the optimal Γ_L changes as well. To account for this changing condition, reconfigurable matching networks are often placed at the PA output which can provide the necessary impedance [4,5]. Additionally, more often than not, the antenna following the output matching network is part of a phased array, and the beam can be electrically steered to focus the main beam in different directions. When this steering takes place, Γ_{ant} also changes, and

impedance matching must be reconfigurable to consistently achieve satisfactory performance [6,7]. The use of finite array information can be used as a baseline for the matching network design [8].

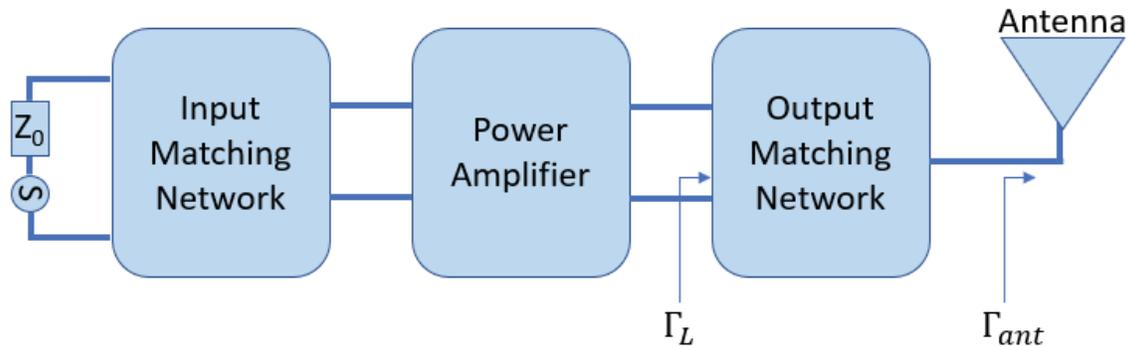


Figure 2.1. Simplified RF power amplifier block diagram.

Distributed Element Matching Networks

Two of the most basic types of impedance matching networks for RF applications are lumped element networks and distributed element networks. “Lumped elements” refer to using actual capacitors and inductors to perform matching, whereas “distributed elements” refer to making use of transmission lines to accomplish the match. The reconfigurable matching network presented in this thesis makes use of distributed elements, specifically microstrip series transmission lines and open-circuit microstrip transmission line stubs. Chosen appropriately, one series transmission line and one open-circuit stub are all that are necessary to transform one impedance into the new, desired impedance at a single selected frequency; such a network is relatively easy to design with the help of the Smith Chart [9,10]. Because the fixed physical length of a transmission line corresponds to different electrical lengths at different frequencies, a distributed-

element matching network will perform differently at different frequencies. Adding additional open-circuit stubs to the transmission line, with the ability to expose or deactivate each one using switching, allows for the creation of a reconfigurable matching network. As the frequency or antenna impedance is changed, the tuner can switch states and change the impedances presented to the PA and antenna based on the operating frequency and which specific stubs are currently exposed.

Impedance Tuner State of the Art

While extensive work has been documented in the area of impedance tuner technology, available options are limited in either power handling or reconfiguration speed, hindering their effectiveness for radar transmitter applications [46].

The problem addressed by this new tuner design, as mentioned earlier, is the tradeoff between power handling and reconfiguration time that has historically existed for impedance tuners. Tuners of varying topology have taken advantage of switches and electrical reconfiguration for over a decade, using a variety of different types of switches, including microelectromechanical systems (MEMS), PIN diodes, custom complementary metal-oxide-semiconductor (CMOS) switches, and varactors; individual contributors are described. Lu [15], Malmqvist [12,13], and Yazdani [18] all designed electrically-tunable reconfigurable matching networks using MEMS switches and capacitors. While MEMS devices provide many RF benefits including beneficial linearity, power consumption, insertion loss, and high frequency performance [15] and can switch on the order of microseconds [40], their power handling is limited to around 25 W for the newest devices [49]. Older devices could handle even less, on the order of single digit watts [15, 23]. Additionally, Hoarau [50] and Sánchez-Pérez [19] utilized varactors as the switching

component for tuners. Similarly, while these devices can switch quickly, their power handling does not exceed 25 W [23, 46], and nonlinearities must also be considered when using varactors [51]. Franco [16] uses custom single-pole single-throw (SPST) switches in a reconfigurable matching network, and while good Smith Chart coverage is achieved, the switches can only handle under 4 W. Nawaz [14] used SiGe transistors as the switching elements, although only low-power test results are discussed, and no time figure is provided. Cai [52] recently used PIN diodes as a part of a reconfigurable PA, and, like the other attempted electrically switchable tuners, the device is projected to handle under 10 W. Plasma technologies have recently been explored for switching, and Vander Missen has experimented with gas plasma in the form of small gas discharge tubes (GDTs), which have more power handling upside, near 50 W, as switches [23]. Semiconductor plasma is also being explored and will be the foundation of the switches used in Chapter Five, and an advantage offered by semiconductor plasma over gas plasma is the fact that the control voltage is independent of the RF signal [40]. While many of these designs have combined fast switches and achieved promising RF coverage with varying topologies including two or more stubs [14,15,17], transformer and capacitive loading [11,12,16], and π -networks [18], the power handling is simply insufficient for many radar systems. Fisher also shows that while the power handling of certain switch varieties has improved, their RF characteristics, particularly insertion loss, linearity, and isolation can also suffer [24].

On the other hand, tuners, commercially available and otherwise, which have shown the ability to handle higher amounts of RF power usually share a common element, mechanical actuation, which limits their potential for quick reconfiguration.

Curutchet [47] describes a coaxial-based high power design demonstrating favorable RF performance but lacks the practical dimensions, weight, and reconfiguration speed desired for new radar applications. This deficiency is common among traditional impedance tuners, such as those produced commercially by Maury Microwave [48] which use a motor to reconfigure and are also bulkier and heavier than practically desirable, although they can handle 250 W. At the moment, Semnani and his team have designed one of the best tuners with reasonable power handling at 50 dBm (100 W), form factor, and a retuning time on the order of hundreds of milliseconds, making use of two mechanical actuators to raise and lower two copper plates [46]. This tuner is the second generation tuner by the team, following a 90 W device which utilized piezo-electric discs for tuning and could be reconfigured on the order of seconds [25].

Impedance Tuning Algorithms

Today, complex systems are increasingly controlled electronically with varying levels of autonomous control. Computer-aided optimization methods have been a topic of interest for decades, and useful techniques can be gleaned from prior work.

Charalambous [17] helps create a foundation for automated optimization techniques.

New techniques are always under development, but contributors have also modified and built upon preexisting techniques, such as Audet [57] extending the pattern search into the mesh adaptive direct search where local exploration is possible. Radar systems are no different, and being able to successfully reconfigure the matching networks to the optimal impedance when operating conditions change is very important. Naturally, this has also been a topic of research for many groups, including teams working with tuners where the reconfigurable elements are switches. Kim describes a greedy algorithm to reconfigure an

RF stub tuner in order to achieve local optima [20]. Wong used a genetic algorithm to optimize an adjustable pi matching network as a solution to half of the problem addressed in this thesis, that is, changing impedance due to antenna array scan angle changing [21]. Smith [22] discusses several algorithm types for a tuner utilizing varactors for antenna matching applications including an exhaustive search, the Hook and Jeeves algorithm, the simplex method, genetic algorithms, and a single-step algorithm which is intentionally light on memory usage. Many algorithms have also been developed for reconfigurable matching networks in general, outside of the switched variety. Cuthbert [54] compares a direct search method with a gradient algorithm with the gradient approach marginally outperforming the direct search. Qiao [55] uses both a genetic algorithm and direct search algorithm with an RF PA consisting of both discrete (MEMS) components and a continuous element (varactor), complicating the search structure. While limited to simulation, Phelps [56] applies a stochastic pattern search to analog circuitry.

The algorithm presented in Chapter Three is different than any of the algorithms currently being applied to switched matching networks and was inspired by the tuner topology (much like the reasoning in [55]), the resulting search space, and empirical testing. Because the search space lends itself to a binary search, the algorithm is more similar to something such as a binary tree search [58]. The need for simplicity is also paramount due to the desire to implement the algorithm on a software-defined radio. The focus is on practicality and converging to a near-optimal state as fast as possible rather than guaranteeing the global optimum is located every single run.

Baylor Team Previous Contributions

The Wireless and Microwave Circuits and Systems (WMCS) research group at Baylor University has been heavily involved in providing solutions to the reconfigurable matching network side of the spectrum sharing solution for the past several years.

On the hardware side, a tuner using varactors has been constructed and tested, two generations of evanescent-mode cavity tuners from Purdue University have been tested, and a test bench centered around a software-defined radio has been developed as a key element for testing and contributing to an effort integrating impedance tuners and associated algorithms in a software-defined radio platform [31-33, 44]. These efforts were focused on optimizing the power-added efficiency (PAE) of the power amplifier in the transmit chain while remaining in compliance with spectral restrictions. Additional work has been performed by Rodriguez-Garcia in an effort to use impedance tuning to lessen the effects of mutual coupling between elements of an antenna array when the beam is steered in a new direction [6-7].

Tuning algorithms have been developed and modified for each of the different types of reconfigurable matching networks used. Algorithms include an interval-halving approach [43] as well as multiple iterations of a gradient algorithm which performs well in the constrained search space [44, 45]. Without the use of any sort of lookup table, the gradient search algorithm for Semnani's second generation tuner was able to converge to the optimal state for PAE while remaining within the spectral boundaries in two to ten seconds [44].

The work described in this thesis examines the design, construction, and testing of a novel high-power reconfigurable matching network, and describes fast tuning

algorithms to optimize these designs in real time. The objective of the optimization is to optimize the output power as the operating frequency and antenna reflection coefficient vary. The initial design of the tuner as well as an overview of the algorithm will be described next in Chapter Three.

CHAPTER THREE

Simulated Design and Algorithm Details

As mentioned in Chapter Two, some reconfigurable matching networks have been shown to be able to handle the high amounts of power required for a radar or electronic warfare (EW) system. Others are able to reconfigure fast enough for pseudo-continuous operation of the system, but both objectives have not been achieved at once. With collaborators examining new designs for state-of-the-art high power RF switches, the idea of using these switches for a future tuner build naturally followed. In preparation for this future tuner, first an RF topology for a switched reconfigurable matching network had to be established and constructed along with a corresponding control algorithm. Here in Chapter Three, the design of the matching circuit topology and algorithm will be explained. Some of the work described in this chapter will be redundant with work presented by Dockendorf, as this portion of the project was a joint effort and is necessary to provide the foundation for the reconfigurable matching network displayed in Chapters Four and Five [27]. Initial simulation algorithm testing was performed entirely by Dockendorf [27], while the RF topology design was a shared effort which was necessary before the boards in Chapters Four and Five were created which were no longer shared tasks.

RF Design and Simulations for Switched Stub Matching Network

When designing the low-power prototype for this switched-stub matching network, there were several design criteria which prompted the decision making for the

device. The first of these criteria was for the reconfigurable matching network to have an octave of tunable bandwidth, that is, for the device to be able to successfully operate as a tuner between 2 and 4 GHz in the radar S-band. Previous testing of tuners in this research group had been in the 3.1-3.5 GHz band.

The next criteria to be met was wide Smith Chart coverage, referring specifically to the tuner's reflection coefficients at both the input and output ports, S_{11} and S_{22} . Rather than take the power amplifier used in the laboratory test bench and one specific antenna array and optimize the design for this one specific toy case, the goal of the design was to spread out the reflection coefficients as well as realistically possible throughout the span of the Smith Chart, allowing the tuner to be useful in a variety of power amplifier and antenna array matching scenarios, as visualized previously in Figure 1.1.

The next requirement for the design was to be able to reconfigure somewhere on the order of nanoseconds or microseconds. As mentioned earlier, fast reconfiguration times would ultimately allow the tuner to support the radar system in continuous operation. Additionally, for shorter term purposes, a very fast possible reconfiguration time would allow the creation and testing of algorithms to showcase this speed in real time and observe whether bottlenecks in the search process are due to the test bench equipment or the tuner itself.

The next requirement follows from that idea, and it is that the tuner must be able to be controlled by a software-defined radio (SDR), as a deployment scenario would include an SDR in place of other heavier, slower RF test equipment commonly used in test benches. For testing purposes, an alternate controlling mechanism was also built in.

The final design criteria, which was outlined in the proposal sent to the Office of Naval Research (ONR), was for the tuner to be as large or smaller than 3" x 4" x 3". This requirement was in place to ensure the design maintains reasonable size, weight, and power (SWaP).

Keysight's Advanced Design System (ADS) was used for the initial RF design and simulations with intentions of designing a matching network meeting the previously mentioned criteria, utilizing switches as the reconfigurable portion, and being feasible to fabricate and test easily. The design began with simple implementation with two ideal switches and two rectangular microstrip open circuit matching stubs. The schematic can be seen in Figure 3.1. Each piece of the main microstrip RF feedline had a characteristic impedance of 50Ω at 3 GHz, the center frequency of the design. These microstrip transmission line pieces also had lengths corresponding to 90° electrical length, again at 3 GHz. The ideal switches had 0 dB of loss with 100 dB of isolation. When the switches are in the "closed" state, the corresponding matching stub is exposed. When the switches are in the "open" state, an open circuit is presented to the feedline. The two stubs originally used had electrical lengths of 90° , $\lambda/4$, at 2 GHz for the stub closer to the input of the tuner and 90° at 4 GHz for the stub closer to the output of the tuner. Many parameters were changed through the design iterations, but the decision to have the larger stubs closer to the input and smaller stubs closer to the output remained in the final design.

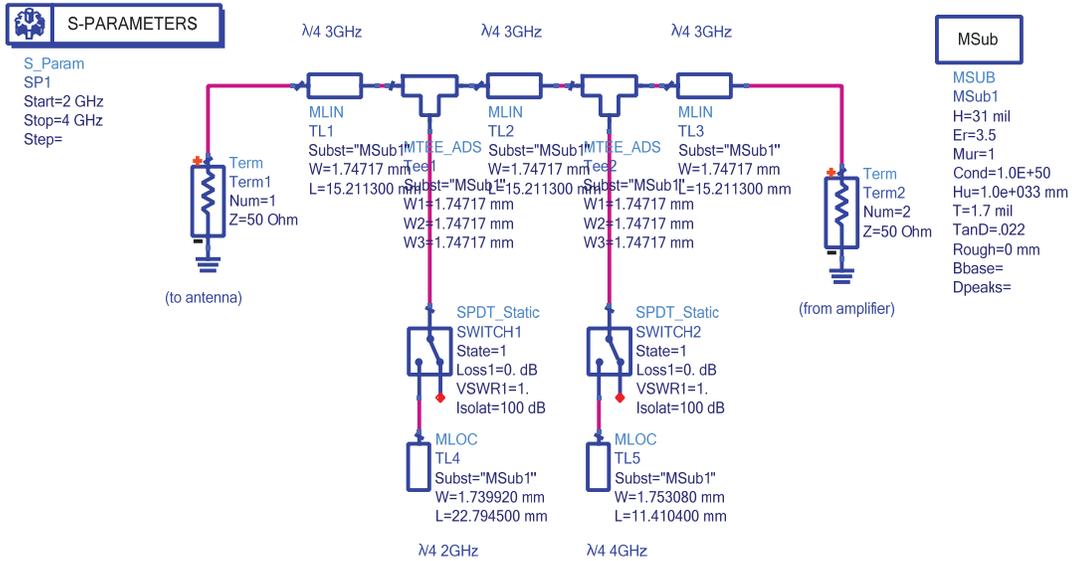


Figure 3.1. Starting point for switched-stub matching network design in ADS.

This simple design was used as a starting point to obtain a better understanding of how changing one parameter would affect the Smith Chart coverage. Figure 3.2 shows S-Parameter sweeps from 2 GHz to 4 GHz for all four possible tuning states for the design, where the tuning states correspond to which switches are open and which switches are closed. The port two reflection coefficients, indicated by the cyan traces (S_{22}) are of primary interest and will be the focus of discussion here, although the port one reflection coefficients, indicated by the red traces (S_{11}) were also observed. On one hand, the initial results confirmed suspicions that with only two switch/stub pairs and four possible tuning states, it was possible to reach three quadrants of the Smith Chart at a given frequency with different states. The results were also informative by the fact that they exposed the reflection coefficient redundancy occurring at 4 GHz specifically due to the $\lambda/4$ stubs, a piece of information helpful for further development of the design.

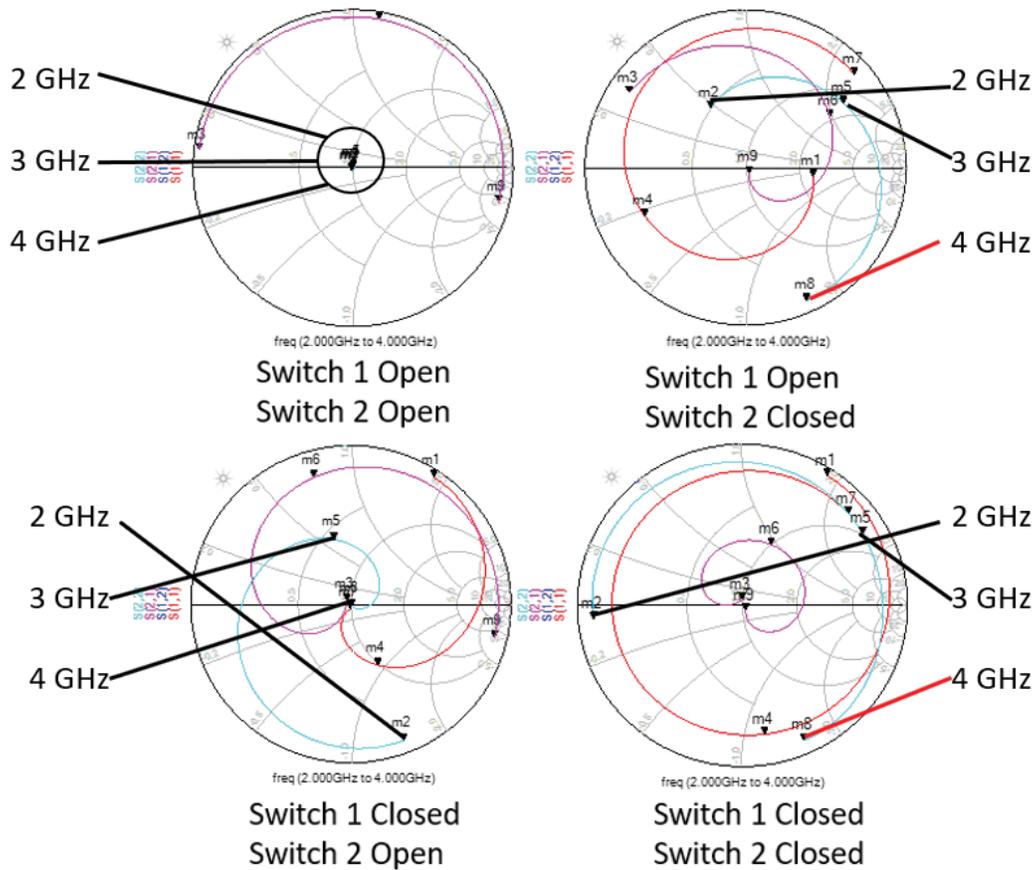


Figure 3.2. S-Parameter traces for simple switched-stub design from 2 GHz to 4 GHz for all four possible tuning states.

This can be seen most clearly looking at the plots for “Switch 1 Open, Switch 2 Closed” and “Switch 1 Closed, Switch 2 Closed”. In both of these instances, the S_{22} value at 4 GHz was essentially identical, noted by “m8” towards the bottom right on the cyan-colored trace. Red lines are present in the figure, indicating that these two points occur at 4 GHz. This redundancy is likely due to the cyclic nature of electrical length and the fact that the two stubs were designed for specific values at 2 GHz and 4 GHz, direct multiples of each other. Ideally, each different switch combination would provide a noticeably different S_{11} and S_{22} to maximize the variety of matching conditions in which the tuner is useful. Notice that the 2 GHz S_{22} for the “Switch 1 Closed, Switch 2 Open”

case is in the same location as the aforementioned 4 GHz points. This is fine, as the other three S_{22} values at 2 GHz are in significantly different locations.

The next steps in the design involved adding more switch/stub pairs, adding actual switch models to the design, and replacing the rectangular microstrip open-circuit stubs with radial alternatives. The rationale behind each of these decisions will be explained prior to showing the design that was developed ultimately.

The number of switched-stubs was increased from two to six. This addition increased the number of possible tuning states from $2^2 = 4$ states to $2^6 = 64$ states. This increase in states both allowed more locations on the Smith Chart to be covered by reflection coefficients and also enabled the to-be-developed algorithm to be utilized in a non-trivial scenario, where a search space actually exists where an intelligent algorithm would perform faster than a simple exhaustive search running through each state and picking the top performer.

The ideal single-pole double-throw (SPDT) switches were replaced with actual simulated models, in the form of .s2p files, for the switches which would be used for the low-power prototype of the switched stub matching network. Two models of the switches were used, one for the open state and one for the closed state. These switches are commercial, off-the-shelf, FET-based devices developed by Analog Technologies. These models were used to provide a more accurate simulation by introducing the actual nonidealities associated with real switches.

The rectangular microstrip open-circuit matching stubs were replaced with radial variations in order to help with the tuner's performance over larger frequency bands which is necessary due to the design goal of an entire octave of tunable bandwidth. A

visual comparison between a rectangular matching stub and a radial matching stub from the top view is shown in Figure 3.3. The geometry here is important. Notice that for the rectangular matching stub, the bottom of the stub is flat. There is one fixed distance for the signal to travel from the top of the stub to the bottom of the stub. Because of this, relatively small frequency transitions would result in the reflection coefficient due to a particular tuner state changing significantly. The bottom of the radial stub is curved; intuitively, there are multiple similar distances for the signal to travel from the top of the stub to the bottom. Because of this curvature, electrical lengths which are not too different can be used for a broader range of frequencies with the same stub. Both the length and the angle of the slanted sides can be adjusted to tune the performance to the desired level.



Figure 3.3. Top view of (left) rectangular matching stub and (right) radial matching stub.

With these three important design decisions in effect, the RF topology was experimentally tuned to the point where the reflection coefficient coverage on the Smith Chart was acceptable. Many elements on the board were given the flexibility to be altered for better performance, including the stub lengths, stub slant angles, and RF feedline length between each matching stub. At first, an analytic method for the built in optimizer

in ADS to use was considered, and parameters such as maximum distance between each reflection coefficient point at each frequency, maximum entropy among the reflection coefficients, and maximum standard deviation between reflection coefficients were tested. None of these methods resulted in satisfactory coverage, instead resulting in situations where the reflection coefficients would clump together or spread out to the very edges of the Smith Chart. For the sake of time, each parameter was hand-tuned iteratively and experimentally with the help of Dockendorf [27] rather than applying a more mathematical approach. Construction feasibility constraints had to be considered when the stubs were designed as well, because early stub size combinations resulting in good Smith Chart coverage resulted in stubs overlapping spatially, necessitating a redesign. The resulting RF topology is shown in Figure 3.4.

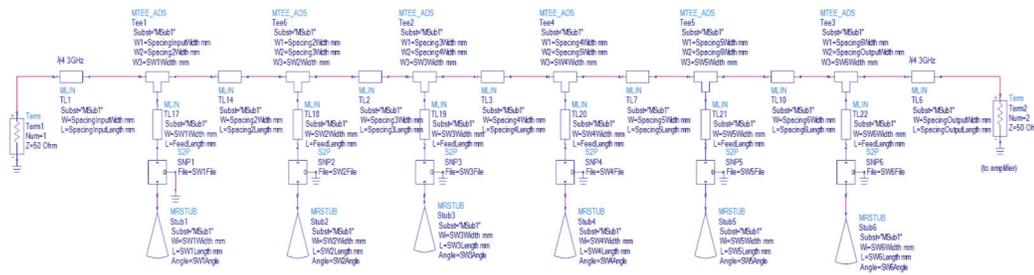


Figure 3.4. Switched-stub tuner RF schematic in Keysight ADS.

The small details in the figure are not important for understanding the results here, as the important changes have been described. The resulting reflection coefficient Smith Chart coverage is shown below in Figures 3.5 and 3.6. Both S_{11} and S_{22} are displayed.

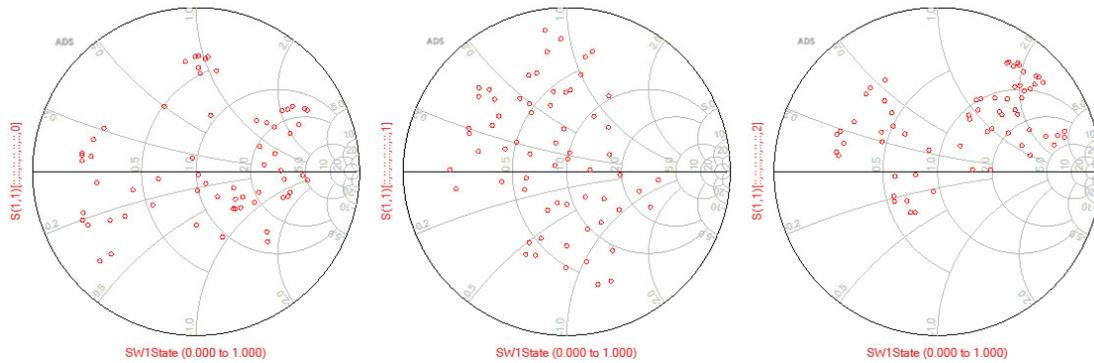


Figure 3.5. S_{11} reflection coefficients in ADS simulation at 2 GHz (left), 3 GHz (middle), and 4 GHz (right).

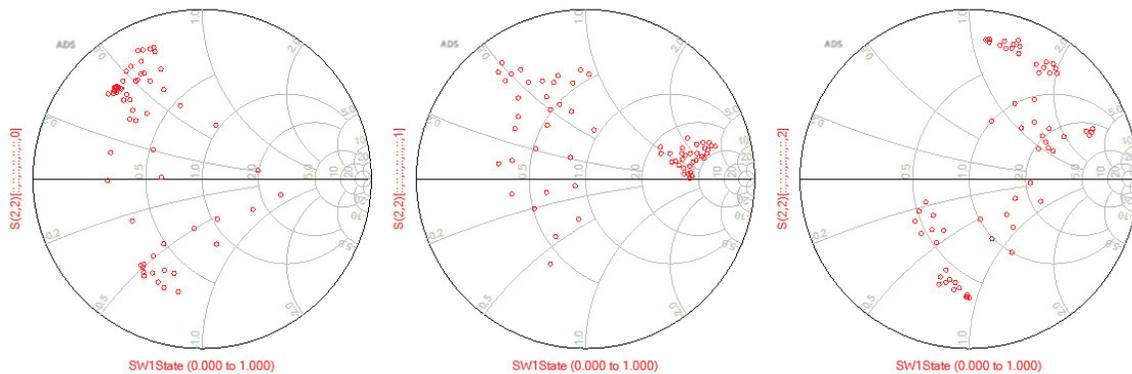


Figure 3.6. S_{22} reflection coefficients in ADS simulation at 2 GHz (left), 3 GHz (middle), and 4 GHz (right).

Notice that, especially for the S_{11} values, solid coverage is achieved in all four quadrants of the Smith Chart at 2 and 3 GHz, and 4 GHz still shows reasonable coverage. The network is not symmetric, so $S_{11} \neq S_{22}$. The reflection coefficients at port one of the network seem to have a better spread, and the plan was to place port one at the load of the PA with port two connected to the antenna. Additional circuitry was added to the board, and it was fabricated and measured. These results will be discussed in Chapter Four.

Algorithm Development for Switched Stub Matching Network

As mentioned prior, the low-power prototype version of the switched-stub reconfigurable matching network was designed in part so that while collaborators worked on designing custom new high power RF switching technologies, the Baylor team could work on creating an algorithm that would work on the low-power prototype tuner as well as other switched-stub tuners with similar topologies and control mechanisms, which were planned to be built once the new switches had reached a certain point in development. Previous search algorithms developed by the WMCS research group had been continuous due to the nature of the search spaces presented by the tuners being used where the domain was dense and small steps could be taken in any given direction. The switched-stub tuner requires an algorithm that takes discrete steps to one of the other 64 possible tuner states. Also recall that, because the design decision was made to utilize six switch/stub pairs instead of two (which would have produced a search space of eight states) an algorithm likely exists which can find the optimal tuner state faster than a simple exhaustive search could. Multiple discrete search algorithms with small differences were drafted with the help of Dockendorf and Egbert and were compared against one another by Dockendorf [27].

The idea behind the algorithm begins with always only retuning to another tuner state that is one Hamming distance away, that is, one bit or one switch away [27]. In order to establish a foundation for this search algorithm, the switch states were represented as six-bit binary values. The most significant bit (MSB) corresponds to the leftmost switch/stub pair, closest to the amplifier. The least significant bit (LSB) corresponds to the rightmost switch/stub pair, closest to the antenna. The middle four bits

are chosen accordingly, MSB to LSB from left to right. This concept is shown in Figure 3.7.

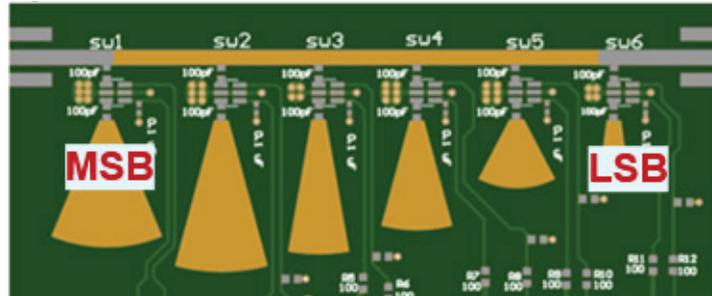


Figure 3.7. MSB to LSB visual.

A binary “1” corresponds to a closed switch, and a binary “0” corresponds to an open switch. The state numbers are often shorted to their decimal representation. For example, state 32 is equivalent to state 100000, which means the leftmost switch is closed and the rest remain open. The algorithm begins by tuning to the starting point for the search, state 0 unless previous search data is used for an optimized starting point for a set of operating conditions. The performance is measured; output power is used to determine the performance of the tuner in current testing. Next, the switch closest to the amplifier is toggled. If the resulting output power is higher than the output power from the initial state, the switch that was toggled keeps its new state, open or closed. Otherwise, that switch returns to its original state. These process of toggling a switch, measuring the output power, and comparing it to the output power of the previous tuner state continues until every switch has been toggled following the most recent performance improvement and no additional improvement is achieved. At this point, the algorithm completes, and the tuner remains at the state with the highest measured output power. Figure 3.8 visualizes this process in a flow chart.

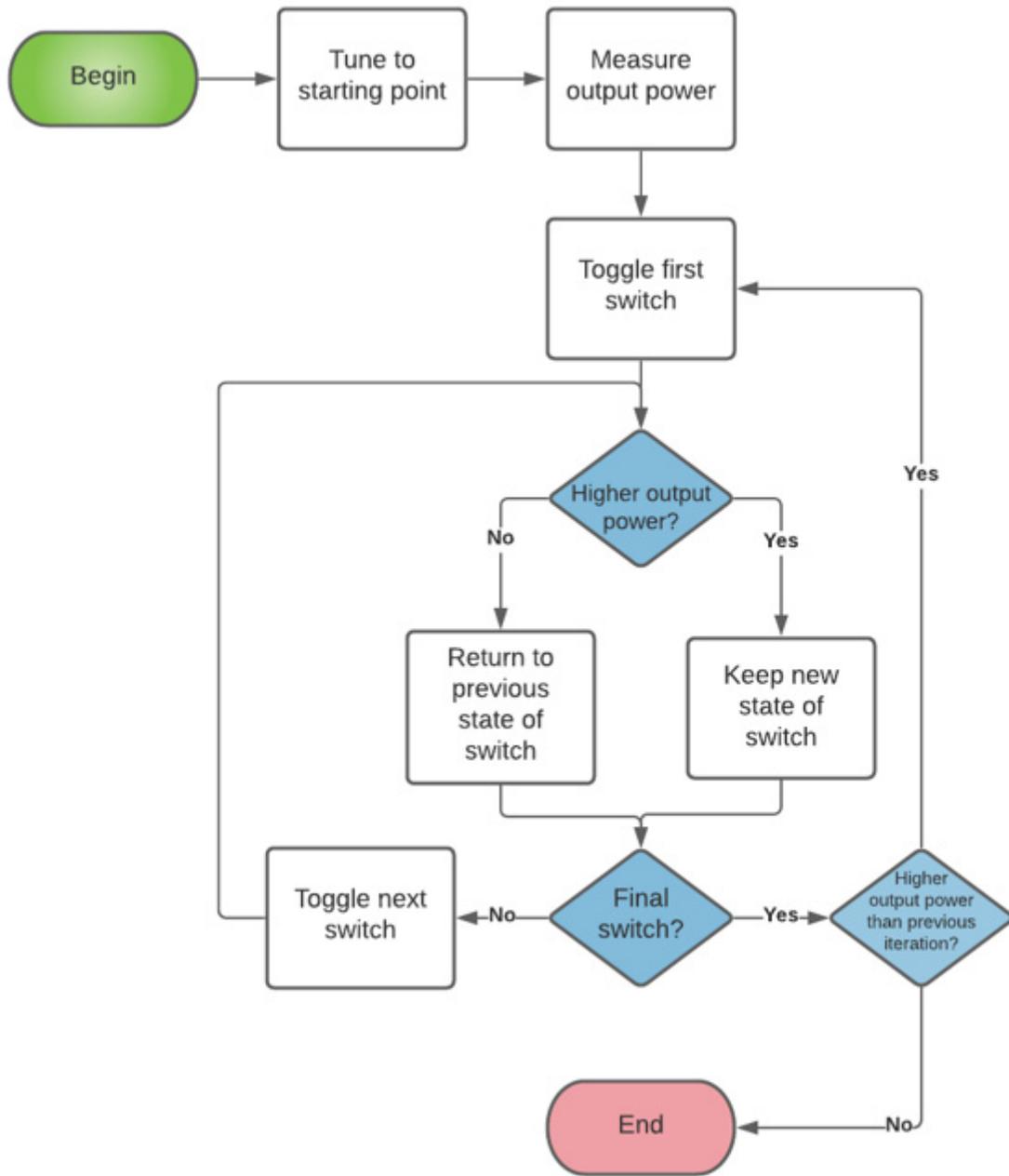


Figure 3.8. Switched-stub tuner reconfiguration algorithm flow chart.

Multiple discrete search algorithms with small differences were drafted with the help of Dockendorf and Egbert and were compared against one another by Dockendorf using a man-in-the-loop, manual approach in ADS, and the described algorithm consistently converged to the optimal tuner state in the fewest number of required measurements [27]. The application and results of this algorithm in both MATLAB and LabVIEW FPGA will be described in Chapters Four and Five.

CHAPTER FOUR

Low-Power Prototype Design, Measurement, and Simulation

The information in this chapter is based on and expands upon the work published in: [28] C. Calabrese, A. Dockendorf, A. Egbert, B. Herrera, C. Baylis and R. J. Marks, "Fast Switched-Stub Impedance Tuner Reconfiguration for Frequency and Beam Agile Radar and Electronic Warfare Applications," 2020 IEEE International Radar Conference (RADAR), Washington, DC, USA, 2020. And in: [29] C. Calabrese, A. Egbert, A. Dockendorf, C. Baylis and R. J. Marks, "Dynamic Online Learning Applied to Fast Switched-Stub Impedance Tuner for Frequency and Load Impedance Agility in Radar Applications," 2020 IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), Waco, TX, USA, 2020.

Following the foundational simulation work described in Chapter Three, the design was implemented, fabricated, and tested. The circuit board described in this chapter is not meant to be any sort of final product but is rather meant to act as a workable version of a switched-stub impedance tuner used to help with algorithm development.

Circuit Board Design Process and Component Analysis

Once satisfactory RF results were obtained using ADS, specifically the reflection coefficients, as described in Chapter Three, the design of the actual circuit board began. Figure 4.1 displays the resulting RF layout from the ADS design.

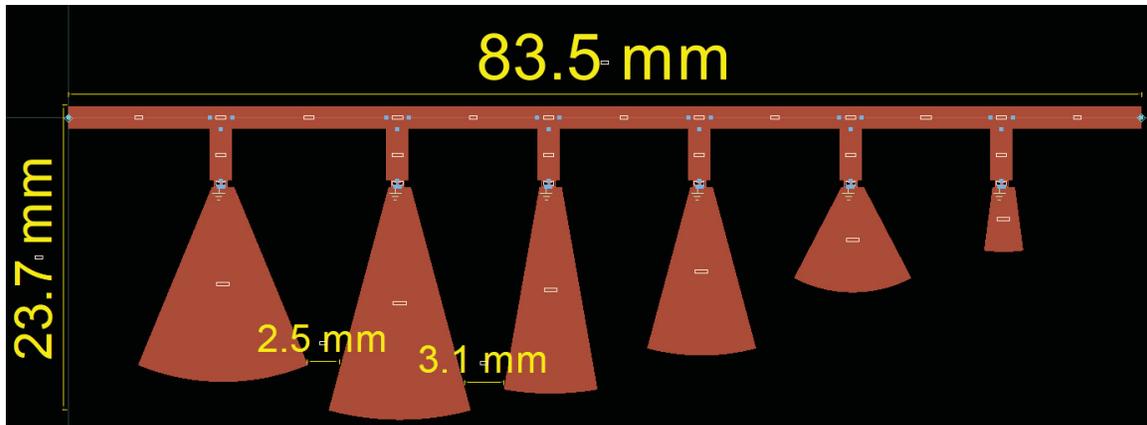


Figure 4.1. RF layout produced in Keysight’s ADS.

The ADS simulation phase was the first step towards meeting two of the design goals, later achieved with measurement data, namely wide Smith Chart coverage and usability between 2 and 4 GHz. The other two goals had to be met specifically by the design of the printed circuit board (PCB). Those two goals were the ability to be controlled by a software-defined radio and a tuner size of 3” x 3” x 4” or smaller. These two design criteria were met, but other practical elements were kept in mind when designing the low-power prototype. Specifically, the design needed to provide a way to power to board, allow the switches to be easily controlled, and allow the device to be controlled by a microcontroller (in addition to the SDR) for ease of debugging and initial testing.

To begin the circuit board design, the first step taken was to export the RF topology from ADS to Altium Designer due to familiarity with the software for this type of design. The features of ADS made this transition relatively seamless. The control and power circuitry was carefully built around the unchanged RF layout. The front and/ back of the resulting PCB in Altium Designer can be seen in Figures 4.2 and 4.3.

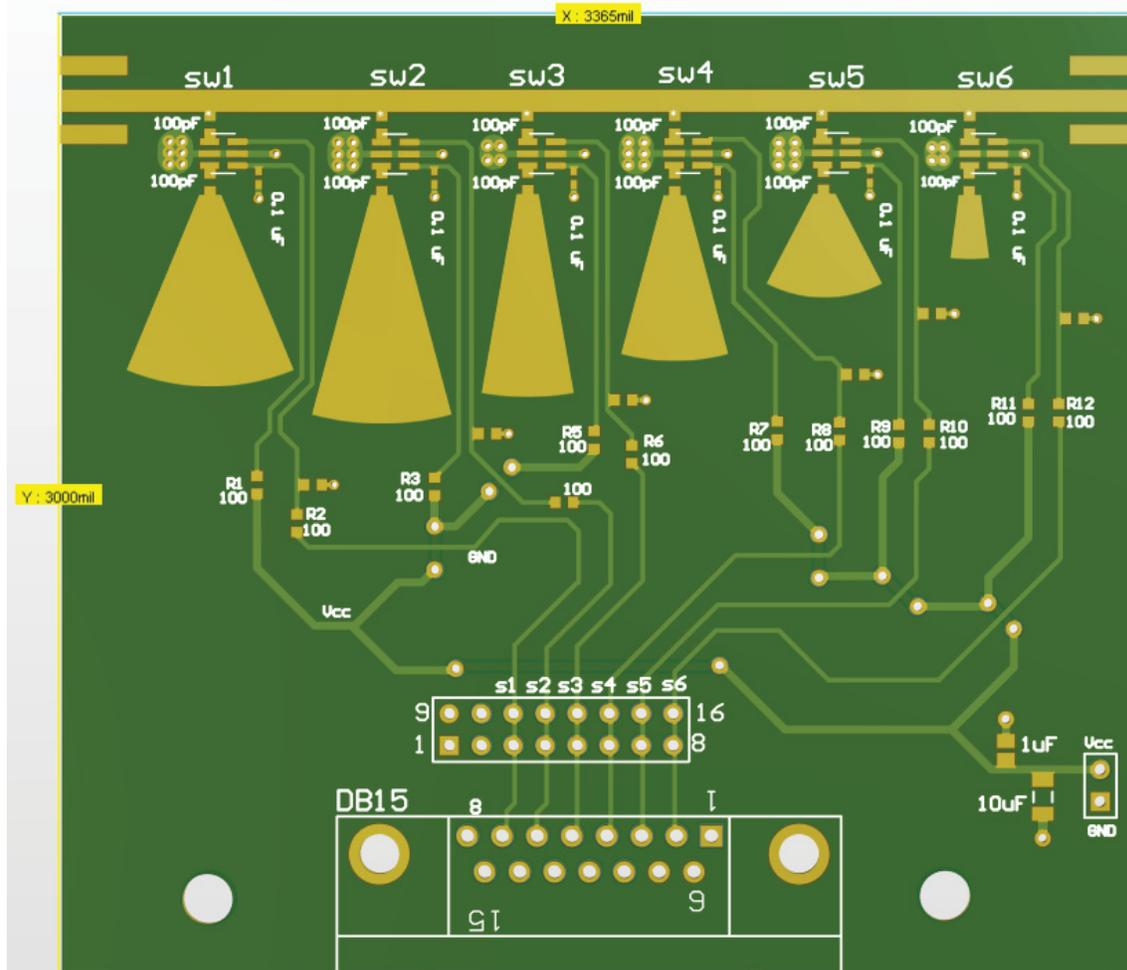


Figure 4.2. Altium design of low-power prototype PCB top layer.

Notice that the x-dimension of the board is 3365 mil (3.365”), and the y-dimension is 3000 mil (3.000”). The 3” x 3” x 4” specification is easily met when the z-dimension, the board thickness, is considered, which is much less than the three inch constraint. In Figure 4.2, above, and Figure 4.3 on the next page, the gold indicates anywhere copper is actually exposed on the layer being shown. In the case of Figure 4.2, this is the top layer’s copper. The traces that can be seen in the lighter green color are also copper on the top layer but are covered with solder mask instead. Holes, as well as

silkscreen markings on the PCB, are shown in white, and the darker green color indicates that there is solder mask present and no top-layer copper.

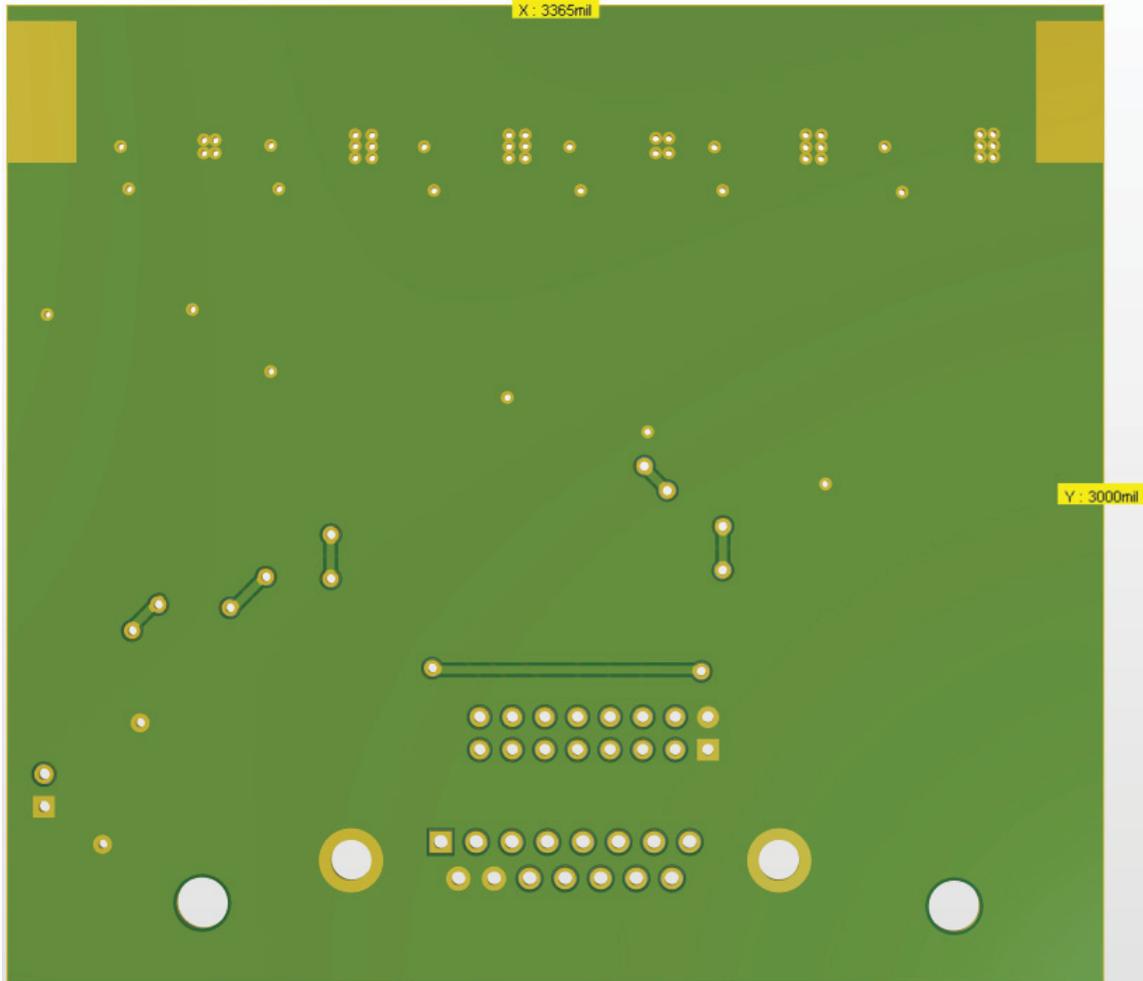


Figure 4.3. Altium design of low-power prototype PCB bottom layer.

The PCB is only a two-layer board, and Figure 4.3 shows the Altium view of the bottom layer of the board. Notice that almost the entire bottom layer is the lighter green color that earlier indicated top-layer copper was present. In this scenario, the lighter green color indicates that bottom-layer copper is present, and it fills almost the entirety of the bottom of the board, because it acts as a ground reference plane for the entire circuit. As

before, gold indicates that copper is on the bottom layer and is exposed instead of covered by the solder mask. An attempt was made to make the signal lines on the top of the board vertical while the ones on the bottom are horizontal and vice-versa in order to minimize the overlap and prevent interference with each other. The bottom of the board was also kept as bare as possible, especially near the area where the stubs were located, in order to avoid splitting up the ground plane. The microstrip simulations were performed under the assumption that the ground plane was sufficiently wide or “infinite”.

Other than the RF topology, the six RF single-pole single-throw switches (9SPST), which are used to expose or hide the radial matching stubs, are likely the most crucial piece of the board design. Figure 4.4 points out these switches, circled in red, on the board.

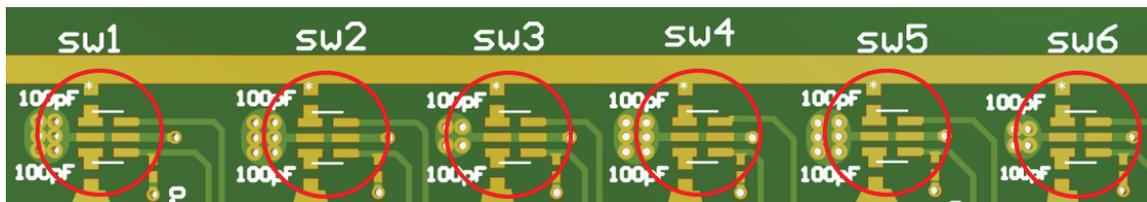


Figure 4.4. Six RF switches circled on PCB.

The low-power FET switches are commercial products designed by Analog Devices for use between DC (0 Hz) and 6 GHz. A simple pinout diagram for one of the switches is shown in Figure 4.5.

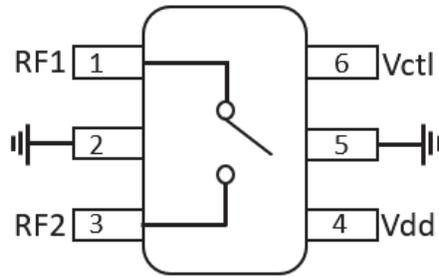


Figure 4.5. Six-pin RF SPST pinout.

The switches can turn on in 20 nanoseconds, turn off in 30 nanoseconds, have an insertion loss of 0.7 dB, a return loss of 20 dB, and have between 12 and 25 dB of isolation depending on the frequency. Referring to Figures 4.4 and 4.5, it can be seen that the RF_1 pin is connected to the main RF feedline with a capacitor, and the RF_2 pin is connected to each respective radial matching stub, also with a capacitor. The capacitors were placed in accordance with the switch's application notes. Additionally, notice that there are groups of four or six vias on a top-layer copper region connected to each switch's left ground pin. These extra vias are in place to provide a lower-resistance path to ground for the signals. The switches are operated by providing power to the V_{dd} pin (either 3.3 V or 5 V) and toggling the V_{ctl} line between 0 V and the value of V_{dd} . When V_{dd} is set, and V_{ctl} is low, the switch is open; when V_{dd} is set, and V_{ctl} is high, the switch is closed. Seen in Figure 4.2, there is a 100 Ω SMD resistor in series on each signal line between the switches' control and power pins and the control and power sources at the bottom and bottom-right of the board. These are current-limiting resistors in place according to the Analog Devices application notes for the switches.

The 16-pin rectangular connector towards the bottom of the board allows a microcontroller to control the board and leaves a row of pins free for probing with a

multimeter or oscilloscope for debugging purposes. Six pins on each row are used for V_{ctl} lines for the switches, one for each switch. One pin on each row creates a common ground reference between the microcontroller, and the final pin on each of the two rows is unused. An Arduino Uno microcontroller was used for initial testing of the board.

The larger connector at the bottom of the board, labeled DB15, provides a connection from the PCB to the front panel of the Ettus X310 software-defined radio which has 12 general purpose input/output (GPIO) pins. The purpose of these pins is essentially identical to the one of the rows of pins for the microcontroller. Six pins are used to connect to the switches' control lines, and one is used to create a common ground reference between the SDR and the tuner.

Looking at the bottom-right of the board, the two-pin power connector can be seen. The board is powered in a simple fashion, as it is just intended to be connected to a benchtop power supply using hooking connectors. The connecting lines are then routed to each power pin of the switches. These power lines as well as the control lines each have at least one decoupling capacitor attached between the respective trace and the ground plane. These capacitors are in place to keep the signals, both power and control, smooth, eliminating ripple that could contribute to incorrect tuner operation. The larger capacitors are placed right next to where the power signal is input into the board to eliminate the larger ripples, and capacitors orders of magnitude smaller are placed closer to the switches to smooth the smaller ripples.

Finally, notice the two lines parallel to the main RF feedline at the top-left and top-right of Figure 4.2 and the gold rectangles in the same locations in Figure 4.3. These pads are in place for soldering the SubMiniature version A (SMA) connectors to the

board which connect to coaxial cables to interface the tuner with the applicable RF equipment in the lab. As is standard for these connectors, the two outer lines on the top as well as the larger pad on the bottom are connected to ground, and the center pin connected to the main RF feed line is for the RF signal.

The fabrication of the boards was outsourced to a professional board manufacturer. The board thickness, 0.031 inches (31 mil) was chosen to match the ADS simulations. FR-4 substrate, with a relative permittivity (ϵ_r) of 4.3 was used, also agreeing with the ADS simulations. The board was constructed, and the complete tuner can be seen in Figure 4.6.

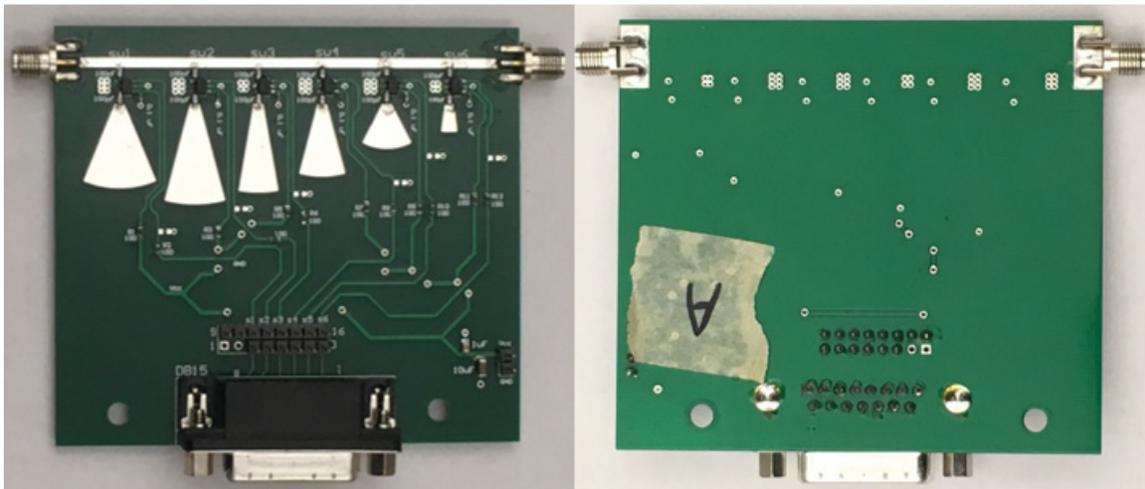


Figure 4.6. Top (left) and bottom (right) of low-power prototype tuner.

Once the boards were in hand, continuity testing was performed to ensure that every electrical node was connected only to the items where it was intended to be connected. After this, the components were added, and actual testing of the tuner began.

Reflection Coefficient Characterization of Low-Power Prototype

After preliminary and precautionary testing to ensure that the board received power correctly, and the switches opened and closed as was anticipated, the first RF testing performed was to take a full characterization of the tuner between 2 and 4 GHz. In this scenario, “characterization” refers to measuring the S-parameter data of the tuner at each of the 64 possible tuner states at each of the frequencies of interest. Similar to the ADS simulations, the three frequencies of primary interest were 2 GHz, 3 GHz, and 4 GHz, but the frequency sweeps on the vector network analyzer (VNA) were taken at 1001 frequency points equally spaced between 2 and 4 GHz. Figure 4.7, below, is the measurement-equivalent of Figure 3.6 which displayed the ADS-simulated S_{11} values of the tuner at 2 GHz, 3GHz, and 4GHz.

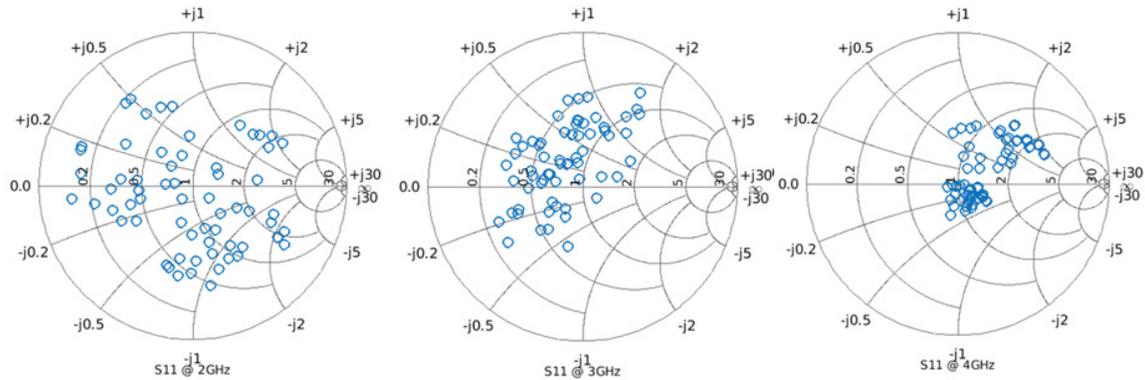


Figure 4.7. S_{11} reflection coefficients from measurement data at 2 GHz (left), 3 GHz (middle), and 4 GHz (right).

The amount of coverage was satisfactory, especially at 2 GHz and 3 GHz. At 4 GHz, the reflection coefficients were more clumped towards the center of the Smith Chart, but the search algorithm still converged to multiple different tuner states at 4 GHz as the optimum when “antenna” reflection coefficient varied. The most obvious

difference between this data and the plots in Figure 3.7 is the rotation of the points on the Smith Chart. This rotation has been attributed to the fact that the coaxial SMA connectors on the board and DC blocking capacitors on either side of the switches were not modeled in ADS, assumed at the time to be built into the switch .s2p files. The SMA connectors add additional length to the RF feed line, among other contributions. This additional length directly correlates with a rotation of reflection coefficients on the Smith Chart. Additional differences are apparent, because the more detailed and more accurate Momentum simulator was not set up or used in ADS. Only the standard circuit S-parameter simulation software was utilized. In continued efforts, Roessler has recently overhauled the model using SMA connectors, capacitors, and the Momentum simulator, confirming these assertions. Overall, the goal of a usable set of reflection coefficients in the frequency band of interest was achieved. Future testing would take advantage of this coverage and demonstrate the tuner's role in PA and antenna matching scenarios.

Power Amplifier Load Matching Algorithmic Optimization Results

Recall Chapter Two where the motivation of the tuner was described. The two matching scenarios specifically mentioned for the tuner included an amplifier and an antenna. This section deals specifically with the PA portion of those motivational goals and tests the frequency agility of the stub tuner. A measurement test bench was built, and the algorithm described in Chapter Three was implemented in MATLAB. Using the Arduino Uno microcontroller, the algorithm communicated with the tuner to present the optimal Γ_L to the PA as the operating frequency of the device changed in the frequency octave.

Before the results can be shown, the test bench where the experiments took place needs to be explained. Figure 4.8 is a photo of the test bench used for the amplifier matching algorithm runs. This is technically the second test bench used for algorithm testing with this tuner. Originally, an RF signal generator and RF power meter were incorporated in the setup to transmit the linear up-chirp waveform and measure the received power, respectively. Once the SDR transmit and receive powers were calibrated accordingly, it replaced both the signal generator and power meter in the setup as a step towards full SDR control. The SDR, labeled “A” in Figure 4.8, is the beginning and end of the loop and acts as the signal generator and power meter, as mentioned. An isolator, labeled “B”, is placed in between the SDR and the rest of the transmit chain in order to protect the SDR from any devices that may become unstable and oscillate, sending large amounts of power back towards the RF transmitter. The Arduino Uno microcontroller, labeled “C”, controls the reconfigurable matching network and is itself controlled serially by MATLAB on the host computer which is not pictured. The device under test (DUT), labeled “D”, is A Microwave Technologies MWT-173 field-effect transistor (FET) the transistor under test. It is biased with $V_{DS} = 4.5 V$ and $V_{GS} = -1.4 V$ with the RF input signal from the SDR having $P_{in} = 14 dBm$. Bias tees can be seen on either side of the DUT. The reconfigurable matching network is next in the chain, labeled “E”. To the left and labeled “F”, the DC power supplies can be seen. The power supply to the right is used to bias the DUT, and the power supply on the left powers the switches on the tuner. The next item in the loop following the tuner is a power splitter. Half of the remaining power is received by the SDR, and the other half is received by the RF power meter,

which plays no role in the algorithm and solely provides visual validation of the power level of the bench at any given moment.

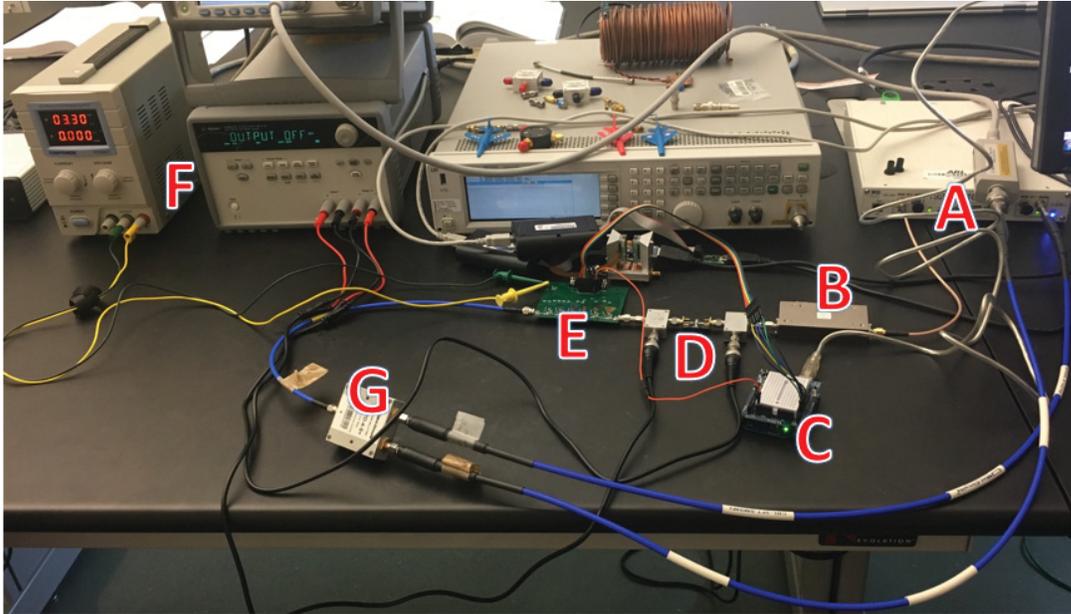


Figure 4.8. Measurement setup: A – software-defined radio, B – isolator, C – microcontroller, D – transistor, E – tuner, F – bias supplies, G – power splitter.

Using this test bench, the algorithm described in Chapter Three was tested. Figure 4.9 displays one example of an algorithm step, with the matching stubs acting as a visual. The tuner begins at state 34 (binary 100010) here and leaves the fifth switch closed due to a performance improvement from whatever the previous state was. The next step is to retune to state 35 by closing the sixth switch. The output power would be remeasured. If an improvement is seen, the sixth switch would remain closed; otherwise, it would be opened. The first switch would then be revisited, and iterations of toggling all switches would continue until a complete pass results in no further power improvements.

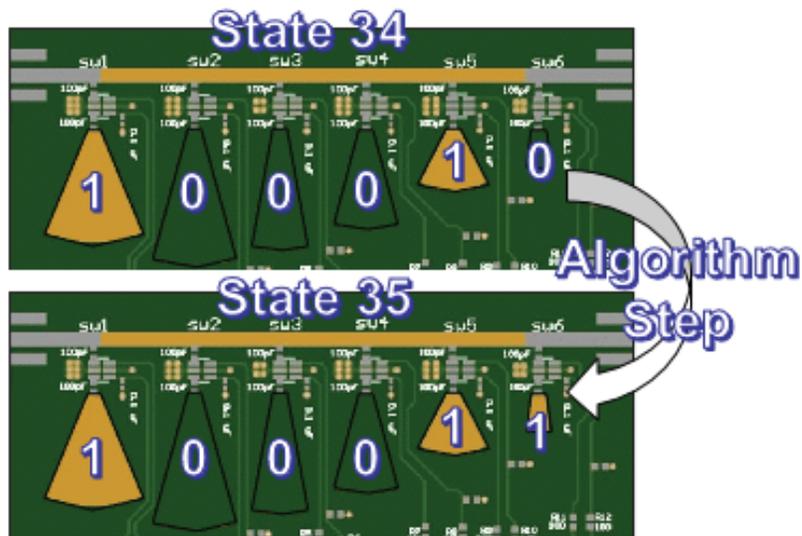


Figure 4.9. Algorithm step visual. Reprinted from [30].

In this test-bench configuration, tuner reconfiguration search algorithms were performed at operating frequencies of 2, 2.5, 3, 3.3, 3.5, and 4 GHz. Figure 4.10 displays the results of one reconfiguration search in terms of power out of the tuner versus time. The output power is meaningful due to the $1/R^4$ relationship between range and radar transmitter power described in Chapter One. Figure 4.11 displays results from the same search on Smith Chart, providing a graphical representation of the steps the algorithm takes from one reflection coefficient to the next and contributing more to the RF rationale of the search steps than only viewing the tuner state numbers and corresponding output powers would otherwise demonstrate.

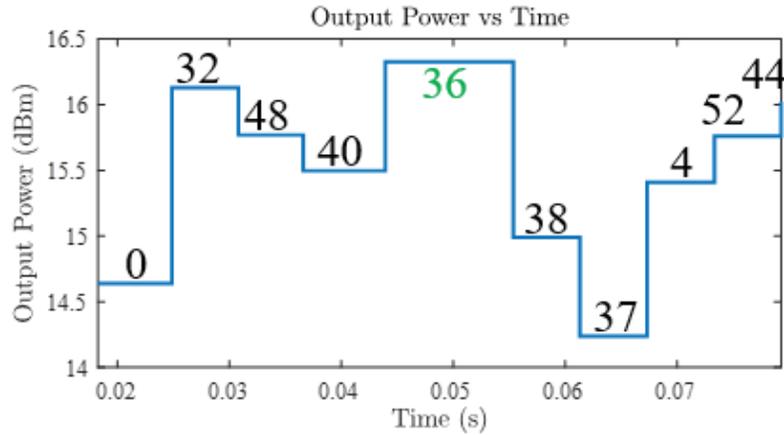


Figure 4.10. Output power versus time plot for reconfiguration search.

The decimal representation of each tuner state is listed above the appropriate output power on the plot. The search was performed at an operating frequency of 3.3 GHz and took 10 measurements to converge to the optimum, state 36 (binary 100100), in roughly 80 milliseconds, achieving an optimal output power of 16.33 dBm. The optimum was found on the fifth measurement, and the algorithm had to perform an additional five measurements to converge.

In Figure 4.11, the reflection coefficient characterization was used to map each of the 10 tuner states to its location on the Smith Chart. The black lines represent states that were measured in the algorithm-based search, the black lines connect consecutive measurement points, the numbers near each measurement point indicate the chronological measurement number, and the red “x” marks the optimum found by the search. The contours in the background represent the results of a load-pull measurement, where the tuner was reconfigured to each of its 64 possible states at 3.3 GHz with the amplifier in the loop. Contours of equal output power were fit to the measured data. It can

be seen that the algorithm correctly converged to a point in the dark red region corresponding to the region of highest output power.

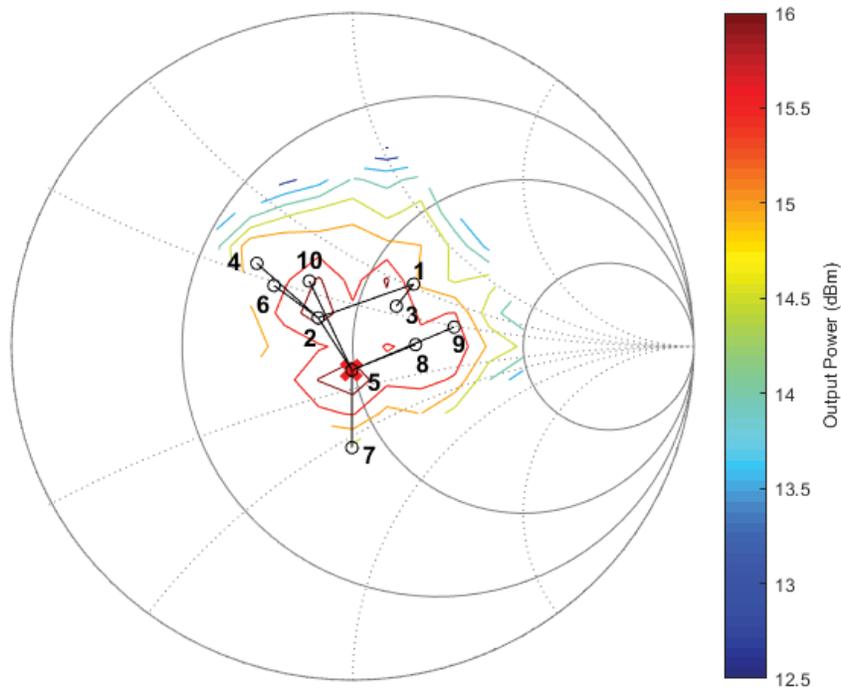


Figure 4.11. Search algorithm progression on Smith Chart at 3.3 GHz.

Additional searches were performed at the other five frequencies mentioned, as the PA's optimal Γ_L changes with operating frequency. As such, it is expected that the optimal state of the tuner will change with operating frequency. Table 4.1 displays the results of these load impedance optimization searches. The tabulated results include the operating frequency, number of measurements taken in the entire search (not just to reach to optimum), time taken for each search to converge, power at the output of the tuner, and the optimal state in each scenario. Each search converged in the 50-80 millisecond range, and this time would eventually be improved by porting the algorithm to the field programmable gate array (FPGA) of the SDR which will be discussed later.

Table 4.1. MWT-173 Γ_L optimization searches for varying operating frequency.

Frequency (GHz)	Number of Measurements	Time (s)	Max Power (dBm)	Best State
2	8	0.0519	17.67	000000 (0)
2.5	8	0.0517	17.77	000000 (0)
3	9	0.0563	17.05	010000 (16)
3.5	10	0.0727	15.84	111000 (56)
4	8	0.0578	13.49	100000 (32)

Observe that the optimal matching state at both 2 GHz and 2.5 GHz is the same, state 0, where every switch is left open. This was not entirely unexpected, because the output power out of the tuner is a combination of the quality of the match between the amplifier and tuner as well as the power lost through the tuner. When a switch is closed, and a stub is exposed, and a certain amount of power loss is incurred. Sometimes the match is good enough to make up for the power lost, but at times a worse match is chosen by the algorithm as the optimal state due to it having a more suitable combination of match and loss. “Loss” is a fairly vague term, and what it means in this scenario is the amount of power absorbed by the tuner, separated from reflections. An intuitive way to look at the total power lost in decibels was desired, and the following equations show the process of arriving at the method of plotting dissipative loss which will be used in this chapter and in Chapter Five. The loss equation begins with the power gain (4.1) equation, previously used in [23, 25], which is simplified due to the assumption of a matched load termination for the tuner.

$$Gain = \frac{|S_{21}|^2}{1 - |S_{11}|^2} \quad (4.1)$$

$|S_{21}|^2$ is the fractional power transmitted, and $1 - |S_{11}|^2$ is the fractional power not reflected. The gain can be converted from linear units to decibels (4.2) by taking 10 times the base 10 logarithm of (4.1).

$$Gain(dB) = 10 * \log_{10} \left(\frac{|S_{21}|^2}{1 - |S_{11}|^2} \right) \quad (4.2)$$

A power gain value is the inverse of a power loss value [53]. The power loss in decibels (4.3) is found by flipping the argument of the logarithm, the original linear power gain expression (4.1).

$$Loss(dB) = 10 * \log_{10} \left(\frac{1 - |S_{11}|^2}{|S_{21}|^2} \right) \quad (4.3)$$

Logarithm properties allow (4.3) to be rewritten as (4.4), negating the value and returning the logarithm argument to (4.1).

$$Loss(dB) = -10 * \log_{10} \left(\frac{|S_{21}|^2}{1 - |S_{11}|^2} \right) \quad (4.4)$$

(4.4) is ultimately used to calculate and plot the power loss. This definition for loss applies assuming the transmit direction of interest is from port one to port two. S_{11} can be replaced with S_{22} , and S_{21} can be replaced by S_{12} if transmission in the opposite direction was being considered. Using the tuner characterization discussed prior which resulted in the reflection coefficients being plotted on the Smith Charts in Figure 4.7, the S-parameters were used to calculate the power loss for each of the 64 matching states across the octave of frequency. The result can be seen in Figure 4.12. Notice that towards the center frequency of the design, 3 GHz, the loss for every single state is around 6 dB or less. On the other hand, near 2 GHz and 4 GHz, there are spikes of loss upwards of 10 dB for some states, nearing 20 dB for the lossiest scenarios. Even if these

states are excellent matches, there is almost zero chance that they will ever be chosen as the optimal state for any scenario. Some of this loss can be attributed to the fact that the tuner topology is based in microstrip which radiates which is why some antennas are made of microstrip. Additional loss can be attributed to the 0.7 dB of insertion loss of the switches themselves. While the loss of some states is definitely greater than desired, continued testing and algorithm development were able to take place successfully. A noticeable ripple is present in each of the loss plots included in Chapters Four and Five which is consistently apparent over many months of measurements. This ripple is consistent over months of measurements and is due to the vector network analyzer test setup used which is carefully calibrated prior to each use. The exact cause is still under investigation. The loss metric will come into play more so in Chapter Five when the custom switches are integrated into the design and adjustments have to be made to accommodate for the larger amounts of power lost.

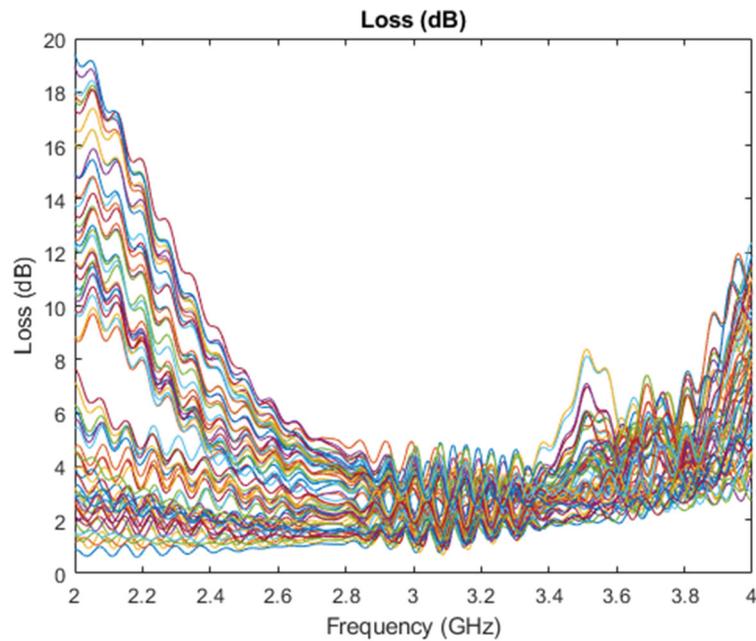


Figure 4.12. Power loss (dB) plotted for all 64 tuner states across 2 GHz bandwidth.

The loss also affects the antenna-only matching scenario as well as the joint PA and antenna matching case.

“Antenna” Matching Algorithmic Optimization Results

The previous section detailed the results of using the low-power prototype switched stub tuner to provide its optimal Γ_L to a transistor in a transmit chain. This section will focus on “beam agility”, matching an antenna only rather without anything else in the loop. This experiment is meant to mimic the fact that as an antenna beam is electrically steered in new directions, the reflection coefficients of each element in the array also change. Instead of integrating an actual antenna array in the measurement setup, a commercially available mechanical impedance tuner from Maury Microwave was used to represent the reflection coefficient of a single element of an antenna array, Γ_{ant} , changing. This Maury tuner is the same device that was used in [36, 37, 38, 39]. A wide characterization of the tuner was performed every 100 MHz between 2 GHz and 4 GHz. The reflection coefficients available for the tuner to be reconfigured to present are displayed on the Smith Chart in Figure 4.13. The chart specifically shows the points available at 2 GHz, but very similar reflection coefficients are able to be achieved at the rest of the frequencies.

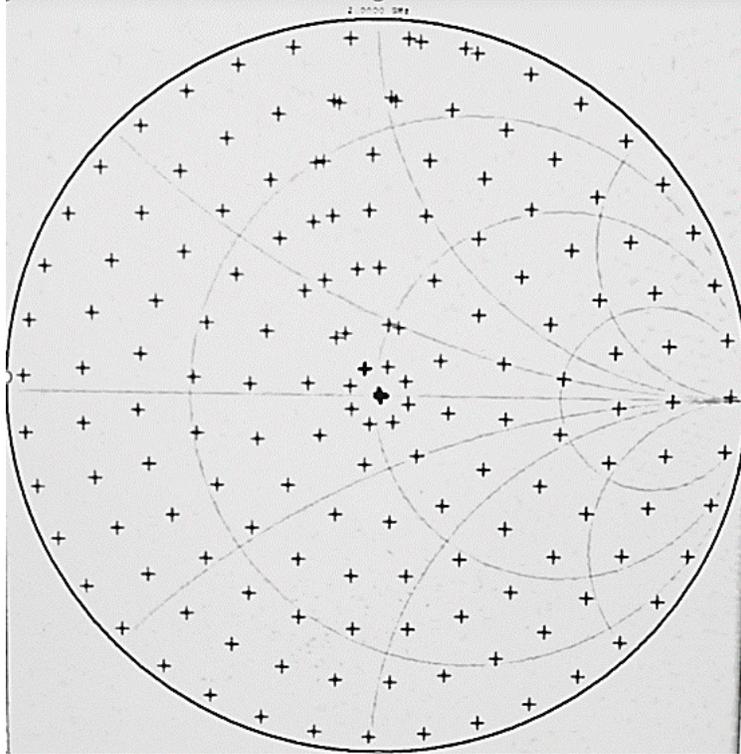


Figure 4.13. Reflection coefficients that Maury “antenna” tuner can achieve at 2 GHz after characterization.

Instead of using the same test bench shown in Figure 4.8, a simple alternate experiment setup was built to use for “antenna” matching algorithm testing while the primary bench was in use. This test setup can be seen in Figure 4.14. A computer controlled VNA is used as both the transmit and receiver. The tuner is placed in between the transmit port of the VNA and port one of the Maury Microwave “antenna” tuner. The VNA transmits a 0 dBm signal, and the same search algorithm is applied, although timing is not considered due to the lengthy measurement time of the VNA. Like in the previous section, the tuner is controlled by a microcontroller which MATLAB communicates with from the host computer.

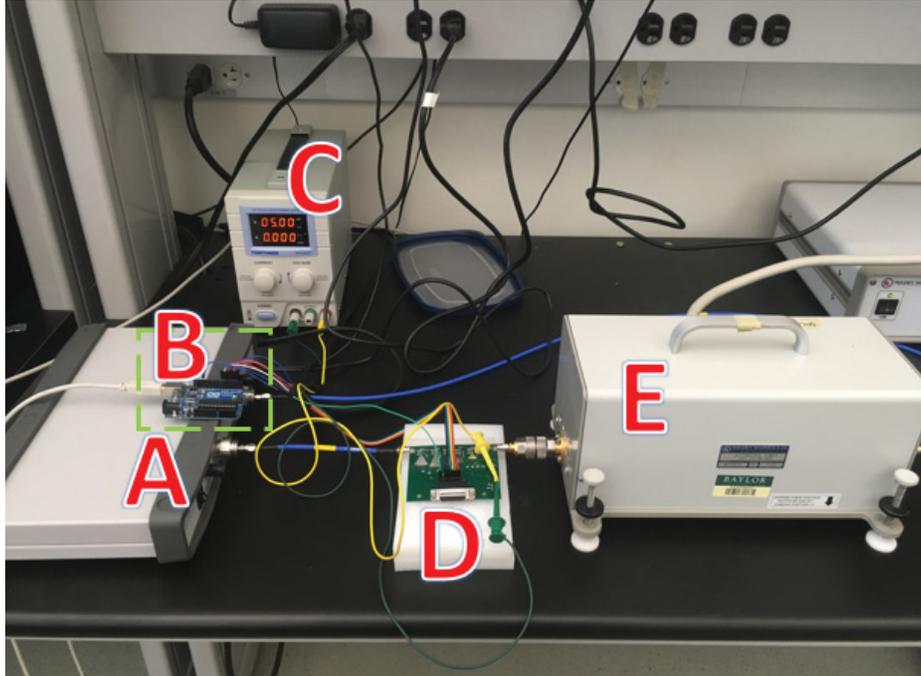


Figure 4.14. “Antenna” matching measurement setup. A – vector network analyzer, B – microcontroller, C – DC bias supply, D – tuner, E – Maury “antenna” tuner.

Before, the items in the measurement loop following the tuner were held constant while the operating frequency of the transmit signal was varied. For the antenna matching experiments, the operating frequency was held constant at 3 GHz and the impedance of the simulated antenna was varied around the Smith Chart. Aside from 0, the reflection coefficients used for testing had magnitudes of 0.25, 0.5, and 0.75. The corresponding angles of the reflection coefficients were 0° , 60° , 120° , -150° , and -30° which are equally spaced 60° apart from each other on a circle. Table 4.2 displays the results of these experiments. Notice that for some of the antenna reflection coefficient values closer to the edges of the Smith Chart, the resulting optimal transmission coefficient is multiple decibels lower than the searches where Γ_{ant} is closer to the center of the chart, due to the match/loss tradeoff discussed earlier. Had the tuner return loss not been incurred in these

instances, there would still be large return loss due to the high magnitude of these antenna reflection coefficients.

Table 4.2. Search results for optimizing output power at 3 GHz while varying Γ_{ant} .

Frequency (GHz)	Γ_{ant}	Number of Measurements	Transmission Coeff. (dB)	Best State
3	0	8	-1.88	110000 (48)
3	0.25/ <u>0°</u>	10	-2.19	000100 (4)
3	0.25/ <u>60°</u>	10	-2.57	100100 (36)
3	0.25/ <u>120°</u>	7	-2.06	100000 (32)
3	0.25/ <u>-150°</u>	7	-1.64	100000 (32))
3	0.25/ <u>-30°</u>	10	-1.81	000100 (4)
3	0.50/ <u>0°</u>	8	-3.06	010000 (16)
3	0.50/ <u>60°</u>	11	-3.45	100110 (38)
3	0.50/ <u>120°</u>	13	-2.55	111000 (56)
3	0.50/ <u>-150°</u>	7	-2.07	100000 (32)
3	0.50/ <u>-30°</u>	8	-2.10	010000 (16)
3	0.75/ <u>0°</u>	8	-5.41	010000 (16)
3	0.75/ <u>60°</u>	11	-5.80	100110 (38)
3	0.75/ <u>120°</u>	13	-4.64	111000 (56)
3	0.75/ <u>-150°</u>	7	-3.91	100000 (32)
3	0.75/ <u>-30°</u>	10	-3.48	010100 (20)

Like the PA optimization searches, none of the antenna matching searches lasted more than two algorithm iterations (thirteen measurements). The 16 different searches performed converged to eight unique tuner states, shown in the final column of the Table 4.2. Other testing was performed involving placing the stub tuner in the opposite orientation with port one of the tuner connected to the Maury tuner which yielded similar results with no orientation greatly outperforming the other. Additionally, testing began to add power lost back into the transmission coefficient measurements in order to influence the algorithm to choose the best match rather than the state providing the best overall transmission coefficient. These experiments did not continue, as a decision was made to focus on the tuner in hand rather than an ideal, lossless version that did not exist.

Combined Power Amplifier and Antenna Matching Algorithmic Optimization Results

After PA matching and “antenna” matching had been performed individually, a measurement setup was constructed in order to match both the PA to the changing antenna impedance, demonstrating the frequency and beam agility of the matching network. In these experiments, both the operating frequency and antenna reflection coefficient were varied, and the search algorithm was required to reconfigure the switched stub tuner to the best state, accounting for both scenarios. Figure 4.15 shows the altered test setup which is essentially the bench from Figure 4.8 with the Maury Microwave tuner inserted after the low-power prototype tuner and before the power splitter.

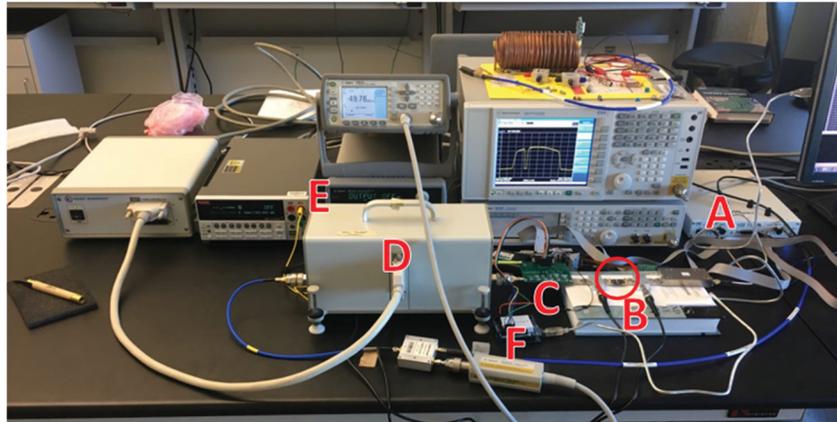


Figure 4.15. Power amplifier and antenna matching measurement setup. A – software-defined radio, B – transistor, C – tuner, D – Maury “antenna” tuner, E – bias supplies.

Fifteen searches were performed in this frequency and beam agile scenario with three searches at 2 GHz, 2.5 GHz, 3 GHz, 3.5 GHz, and 4 GHz each and the closest Maury tuner reflection coefficients to 0, $0.5 \angle -90^\circ$, and $0.75 \angle 120^\circ$ at each frequency. The results for this experiment can be seen in Table 4.3.

Table 4.3. Search results for optimizing power out of tuner as operating frequency and simulated antenna reflection coefficient vary.

Frequency (GHz)	Γ_{ant}	Number of Measurements	Time (s)	Max Power (dBm)	Best State
2	0.04 / 24°	8	0.0704	12.85	100000
2	0.54 / -91°	8	0.0598	12.89	000000
2	0.69 / 121°	8	0.0701	12.93	000000
2.5	0.10 / 70°	13	0.0934	12.80	000010
2.5	0.47 / -81°	8	0.0648	13.20	000000
2.5	0.69 / 119°	8	0.0603	13.20	000000
3	0.09 / 20°	8	0.0644	12.62	000000
3	0.46 / -87°	15	0.0792	12.07	000101
3	0.78 / 118°	15	0.1125	12.03	000101
3.5	0.06 / 68°	10	0.082	11.84	111000
3.5	0.59 / -93°	11	0.0825	9.69	110100
3.5	0.69 / 115°	13	0.1032	10.77	111001
4	0.06 / -47°	13	0.0934	9.59	100001
4	0.50 / -92°	13	0.0884	9.60	100001
4	0.69 / 122°	12	0.0903	6.99	100010

The results are similar to those of the previous scenarios. Some of the searches took slightly longer, converging in three algorithm iterations (15 measurements) and in as many as 113 milliseconds. As seen before in the amplifier matching scenario, output power suffers towards the upper end of the frequency band due to less power being available to the tuner and many tuner states being more lossy near 4 GHz. This experiment was the final test desired before performing more significant alterations to the test bench and SDR platform.

Optimization Search Speed Improvements with Software Defined Radio Control

Once each of the desired matching scenarios had been examined and algorithm errors had been diagnosed and corrected, the goal became to optimize the algorithm itself. This meant that instead of running the search algorithm on the host computer and

using the microcontroller to communicate with the tuner, the SDR would both need to run the algorithm and perform the communication with the tuner directly. Egbert used LabVIEW FPGA to rewrite and compile the algorithm on the FPGA of the SDR. He also developed a simple LabVIEW frontend to control the tuner. The measurement system is described in [35]. Cutting out the involvement of the host computer in the search algorithm as well as the no longer necessary communication links was able to reduce the time needed for a single tuning operation from 5.23 ms to 1.88 μ s (with sub operations taking tens to hundreds of nanoseconds), three orders of magnitude of improvement. The time needed to complete an entire optimization search dropped from tens of milliseconds to as low as 13.1 microseconds if the tuner optimum was located in the first iteration of the algorithm. These time figures are based on the 100-sample pulsed waveform transmitted by the SDR. If the number of samples is increased, the time necessary for the search to complete is also increased. The choice of the RF switches influenced the reconfiguration time significantly, as the 20-30 ns switching time allowed the SDR's high speed capabilities to be fully utilized. With the hardware optimized, one final idea was implemented to attempt to decrease the average search time even further within the SDR platform.

Starting Point Dynamic Learning Applied to Tuner Optimization Algorithm

In the SDR platform, searches have the ability to converge within 13.1 μ s, however, depending on the specific operating conditions of the search, some searches would last two or three times longer, due to the optimal state requiring multiple switches to be closed, resulting in additional measurements being taken. Up to this point, every search had began at state 0, all switches open. Using a dynamic lookup table to learn

tuner optima for given sets of operating conditions was able to decrease the average search time necessary. Figure 4.16 shows the test bench used for this additional algorithm testing. Notice that the setup is the same as the one shown in Figure 4.15, however the microcontroller is no longer in use, and the tuner is being controlled by the SDR.

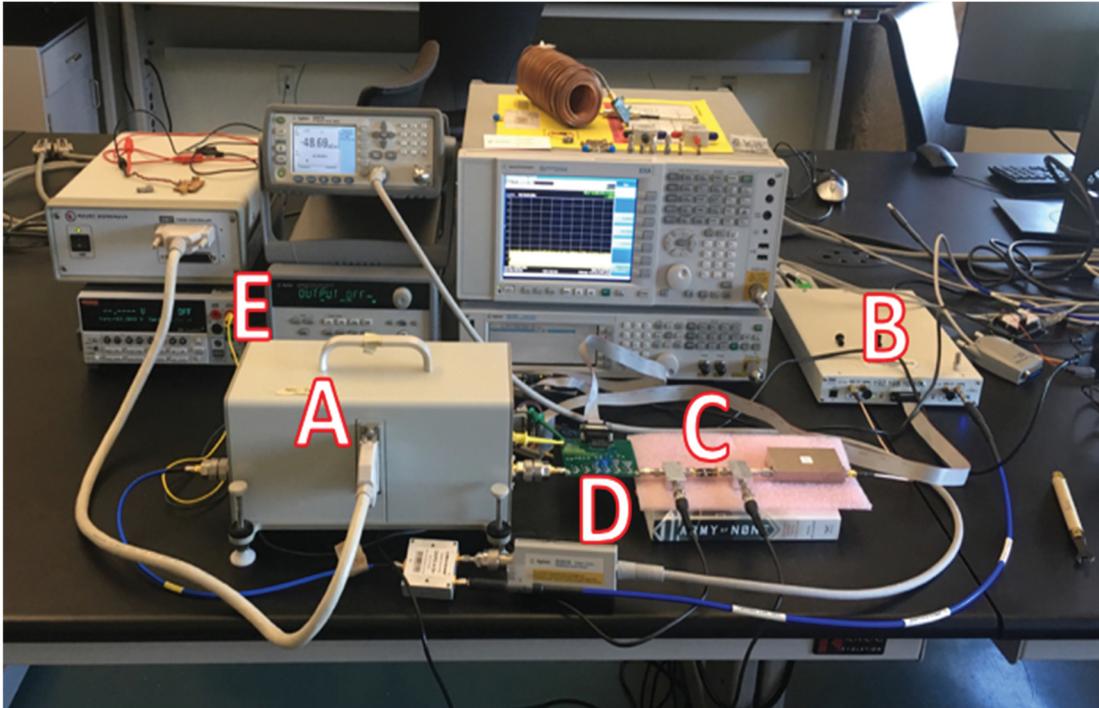


Figure 4.16. SDR-controlled algorithm test bench. A – Maury “antenna” tuner, B – software defined radio, C – transistor, D – tuner, E – bias supplies

As before, the frequencies used for this testing are the same five frequencies between 2 GHz and 4 GHz, spaced 500 MHz apart to span the octave. The five Γ_{ant} values used for this experiment are 0, $0.5 / \underline{45^\circ}$, $0.3 / \underline{120^\circ}$, $0.65 / \underline{240^\circ}$, and $0.4 / \underline{310^\circ}$. These “antenna” reflection coefficients, with one in the center of the Smith Chart and the others in each of its four quadrants, were chosen in order to demonstrate the robustness of the tuner as operating conditions vary. The reflection coefficients can be seen visually on

a Smith Chart in Figure 4.17. These selections provide 25 unique sets of operating conditions, five frequencies and five reflection coefficients.

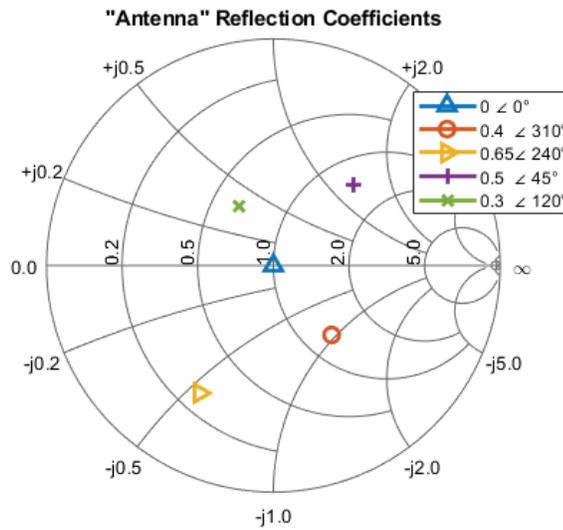


Figure 4.17. Five “antenna” reflection coefficients used for starting point dynamic learning searches.

Previously, Dockendorf performed optimizations using previous search results using Semnani’s mechanically actuated, continuous impedance tuner [34]. In those optimizations, the search would generally converge to a point nearby the starting point. The hope for taking advantage of previous search results with the discrete stub tuner is that searches would converge to the starting point every time.

The experiment was set up such that the order 25 possible pairs of operating frequencies and antenna reflection coefficients would be randomized, and a search would be performed at each pair, starting at state 0, and logging the optima. The order of the operating condition pairs was randomized again, and the searches were performed again. This time, the algorithm recalled the previous optimal states and used them as the starting

points for the new searches. In a more realistic scenario, the antenna element reflection coefficients would be unknown, but these could be replaced functionally with the array scan angle. Table 4.4 shows the results of a search taken at 3.5 GHz with the Maury tuner's reflection coefficient set at 0.4 /310^o; the search begins with all switches open. Table 4.5 shows the results of a search with the same set of operating conditions, starting at the optimum found previously.

Table 4.4. Search performed without previous starting point information.

Tuner State	Output Power (dBm)	Time Taken (us)
0	12.73	1.870
32	15.99	3.745
48	20.55	5.625
56	19.79	7.505
52	22.23	9.385
54	20.51	11.265
53	19.54	13.145
20	20.18	15.025
36	16.05	16.905
60	22.34	18.785
62	19.45	20.670
61	21.11	22.550
28	19.18	24.430
44	16.35	26.310

The search converged to state 60 and required 14 measurements, completing in 26.3 μ s. In contrast, the search beginning at state 60 still converged to state 60, required seven measurements, and lasted 13.1 μ s, saving half of the time necessary to perform the search. Not every set of operating conditions saved this many measurements, but this example provided a good demonstration of the impact of starting point optimization that was intended when the experiments began.

Table 4.5. Search performed with previous starting point information.

Tuner State	Output Power (dBm)	Time Taken (us)
60	22.27	1.870
28	19.13	3.745
44	16.41	5.625
52	22.24	7.505
56	19.83	9.385
62	19.47	11.265
61	21.12	13.145

Table 4.6 provides a summary of the results from all 50 searches performed for the experiment, half with and half without taking advantage of the dynamically learned starting points.

Table 4.6. Starting point optimization results summary.

Average Search Completion Time Without Memory (μ s)	Average Search Completion Time With Memory (μ s)	Average Number of Measurements Without Memory	Average Number of Measurements With Memory	Percentage of Repeat Optimal States (%)	Percent Time Savings (%)
17.8	13.1	9.48	7.2	80	26

The algorithm runs which utilized the previous search optima averaged more than two fewer measurements per search and resulted in a 26% decrease in time needed for a search to converge, on average. While the hardware could not be pushed much further in terms of time savings, these additional improvements to algorithm completion time are significant.

CHAPTER FIVE

Semiconductor Plasma/Laser Diode Prototype Design, Measurement, and Optimization

The information presented in this chapter is based on and expands upon the work presented in [30]: C. Calabrese, J. Roessler, A. Egbert, A. Fisher, C. Baylis, Z. Vander Missen, M. Abu Khater, D. Peroulis and R. J. Marks, “A Plasma-Switch Impedance Tuner for Real-Time, Frequency-Agile, High-Power Radar Transmitter Reconfiguration,” 2021 IEEE MTT-S International Microwave Symposium, Atlanta, GA, June 2021.

When satisfactory algorithm results had been obtained with the low-power prototype and collaborators had demonstrated sufficient success with switching technologies, work began on the next tuner prototype.

Laser Diode/Silicon Chiplet Switch Description

Before the new tuner design is discussed, the main difference between this tuner and the one described in Chapter Four must be introduced and described. This difference is the switching mechanism. Recall that previously, off-the-shelf low-power FET switches were used. The new switches consist of two primary elements; these are the silicon chiplets which are attached to the RF board between the feedline and the stubs. They are the part of the switch that, when excited, close and expose the corresponding matching stub. The other part of the switch actually performs the excitation; this is the laser diode. The principles behind the switching operation are detailed by Fisher [24]. The chiplets have conducting surfaces on either side of a small gap where the laser impinges, with a simple diagram of a chiplet as if viewed from the side can be seen in Figure 5.1. Illuminating the silicon chiplets with a laser allows the photons to create electron hole pairs and is more effective when higher power lasers are utilized. More

electron-hole pairs essentially complete the circuit, closing the switch. Testing by Fisher was performed between 0.008 W and 1.5 W of laser power using a fiber-coupled laser with a 100 μm fiber diameter, allowing very concentrated, precise illumination of the gap on the chiplet. Because of financial motivations and the desire for portability, the tuner was constructed with six \$25, PCB-mountable, 0.5 W laser diodes rather than multi-thousand dollar fiber coupled laser devices.

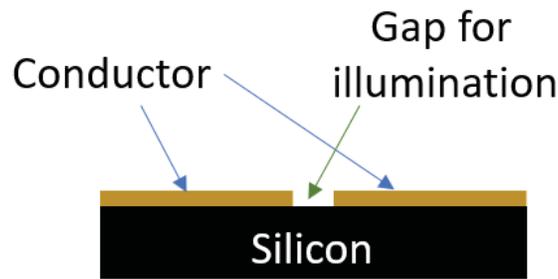


Figure 5.1. Simplistic visualization of the chiplet half of the switch.

Once the diodes and chiplets were chosen, many of the variables impacting switching performance became fixed. In [24] Fisher presents an equation (5.1) describing the number of excited carriers in the gap.

$$n(z) = \eta\alpha\tau \frac{P\lambda}{Ahc} \frac{1-R}{1-\alpha^2L^2} \left[e^{-\alpha z} - \frac{\alpha L^2 + v_s\tau}{L + v_s\tau} e^{-\frac{z}{L}} \right] \quad (5.1)$$

Many of these parameters would have been difficult to change with the preexisting design, but one significant element to the design that can change, however, is the laser power density incident on the chiplet gap. This is indicated by P/A in the second term of (5.1), where P is the power of the laser diode and A is the area where the light is incident. As was mentioned prior, higher incident power levels result in the device behaving closer what would be considered an ideal (closed) RF switch, improving significantly in both

insertion loss and return loss and decreasing the equivalent resistance of the switch. Initial testing of the laser diode/silicon chiplet switches on a tuner device, which will be detailed in this chapter, indicated that the light emitted from the diode diffused too quickly for satisfactory RF performance. Aside from major design changes, the best method to fix this issue was the integration of microlenses into the design. The lenses are placed flush against the chiplets. While perhaps not the exact optimal distance, this does not allow the light to converge to a focal point which, when fabrication equipment lacks the necessary precision, would likely miss the gap of the chiplet altogether. As a 100 μm laser spot size was used in the initial testing with the fiber coupled laser, a good data point was provided regarding an effective laser spot and power density. Tuner results with the inclusion of the lenses in the design will be shown as well later this chapter.

These joint laser diode/silicon chiplet switches would replace the low-power FET switches used for the results shown in Chapter Four and necessitate somewhat of a redesign. Of course, the control circuitry would need to be replaced to control the laser diodes instead of the FET switches, but due to the orientation necessary for the laser diodes and silicon chiplets to interact properly, the tuner design split into two boards rather than one.

Circuit Board Design Process and Component Analysis

The inclusion of the new type of switches in the design required a more creative orientation of parts than the board simply laid out in two layers as was the case for the low-power prototype. The tuner was split into two boards. One PCB, referred to as the “control board”, was created for the six laser diodes to be powered and allows control of the diodes by a microcontroller or an SDR, just like the low-power prototype. The second

PCB, referred to as the “RF board”, is a smaller board consisting of the same six microstrip radial matching stubs as used before as well as the six silicon chiplets described prior and six vias directly underneath the gap in the chiplets to allow illumination. Larger vias were added to each board, aligned with each other, in order for the boards to be aligned with one another correctly and allow for the boards to be connected. Altium Designer was used for these designs as well, and one of the boards needed to be flipped and rotated 180° in order for this alignment to be correctly achieved before fabrication. Figures 5.2 and 5.3 show the front and back views, respectively, of the control board. The colors explained in Chapter Four are representative of the same regions of the board in this case. Some of the key components on the control board will be discussed following the images.

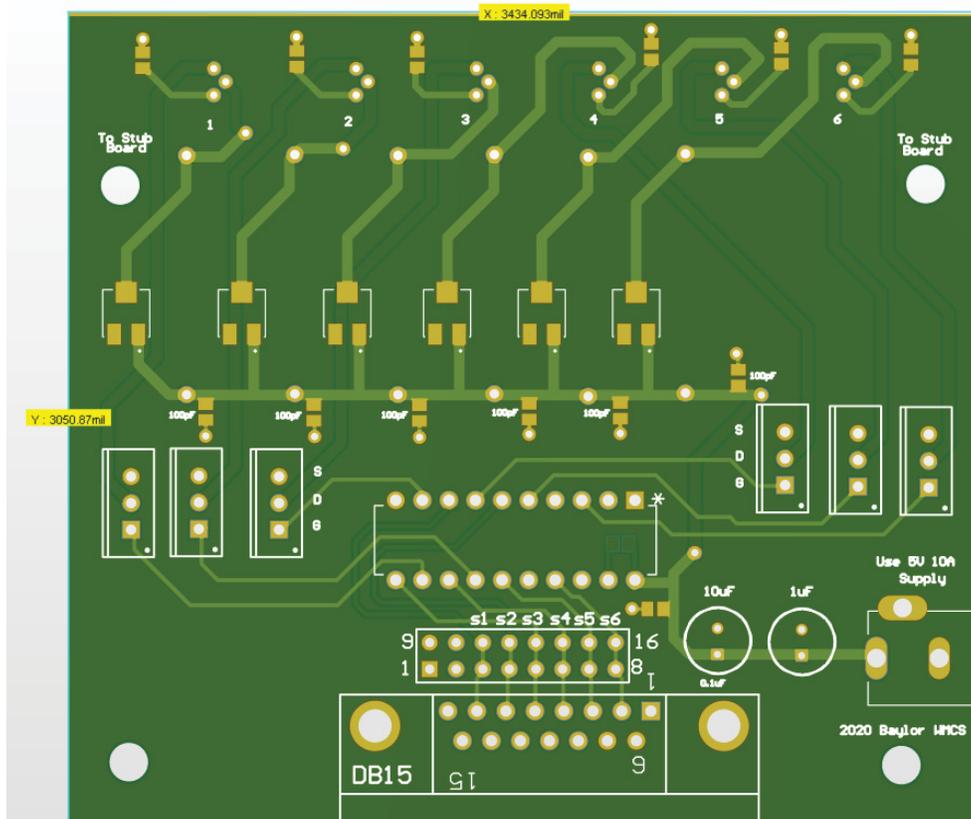


Figure 5.2. Top layer of laser diode tuner design control board in Altium.

The control signals for the laser diodes originate at the bottom of the board from either the DB15 connector or the 16-pin connector for microcontroller jumper wires directly above that, similarly to the FET switch signals on the low-power prototype. Unlike the low-power prototype, the signals then pass through the 20-pin digital buffer which is in place to protect the controlling device, the microcontroller or especially the SDR, from any accidental, excess current sourcing or sinking. Each of the six signals from the digital buffer is connected to the gate of one of the six FETs, towards the middle of the board, marked by vertical rectangles and the letters “S”, “D”, and “G” on the inner two components. The FETs act as switches, drivers for the lasers that can actually handle the power drawn by the diodes, shown in the Figure 5.4 diagram.

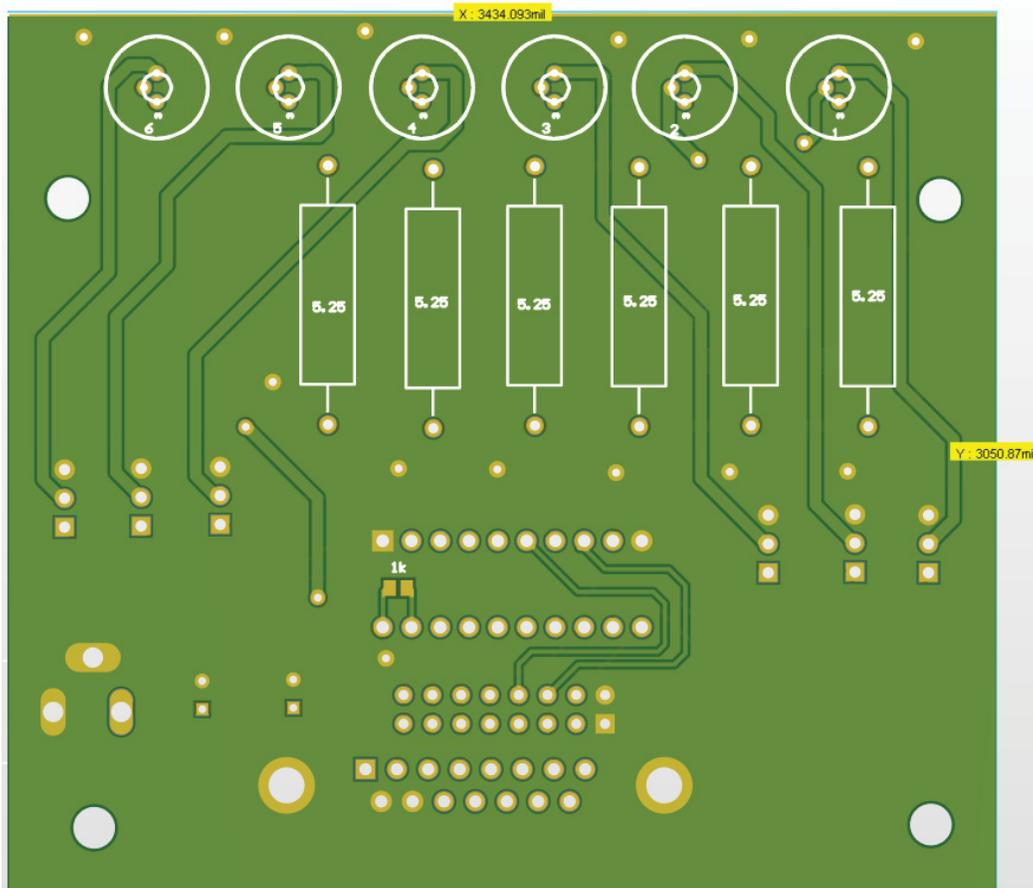


Figure 5.3. Bottom layer of laser diode tuner design control board in Altium.

The higher power source for the diodes originates at the three-pin power jack at the bottom right of the board. A 5 V, 10 A DC power supply is used, sufficient to power each 0.5 W laser diode at once, and decoupling and smoothing capacitors are placed near the power jack input and near the input of each parallel resistor combination. Trimmer potentiometers (three-pad components towards the middle of the top layer of the board) and larger power resistors (labeled “5.25”) on the bottom layer of the board are in place to set the amount of current delivered to the laser diodes when the FETs are switched “on”. The trimmers are placed in parallel with the power resistors and serve only to adjust the power if there are discrepancies between the amount of power delivered to each diode. The laser diodes can be seen at the top of the bottom layer of the board, indicated by the six pads drawn as concentric circles with three pins each. The four larger holes, oriented near each corner of the board, are in place to align the control board with the RF board and to mount the tuner in a housing which designed by Egbert and used to contain stray beams for safety purposes.

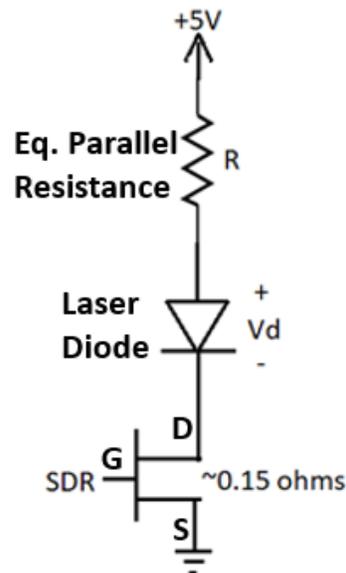


Figure 5.4. FET diode driver schematic.

The trimmer/resistor parallel combination, laser diode, and drain to source channel of the FET are all in series. The SDR (or microcontroller) provides the high signal necessary to close the FET switch, and then current flows in accordance with the amount of resistance chosen. A 5.25Ω resistor was chosen based on equation (5.2) with the goal of setting the current through the laser diode to 650 mA or below. V_d , the forward voltage of the diode was specified on the datasheet to be between 1.6 V and 2.2 V.

$$I = \frac{5 V - V_d}{R + 0.15 \Omega} \quad (5.2)$$

The drain-source resistance of the FETs is roughly 0.15Ω , when they act as closed switches. The edge cases, 1.6 V and 2.2 V were inserted for V_d , and current was calculated to be 630 mA if the forward voltage is 1.6 V and 580 mA if the forward voltage is 2.2 V. These current values allow the diodes to operate at near max rated power while remaining safe. Notice that the diodes are meant to be mounted on the bottom layer of the control board, meaning that they will illuminate downwards. This design choice allows meaningful components, such as connectors, pins for probing, and trimmer resistors to be easily accessible on the top of the board, even when the tuner sits in its housing, with the control board and RF board connected. The Altium designs for the top and bottom of the RF board are shown in Figure 5.5. Notice that the main RF feedline and stubs use the same layout as previously seen on the low-power prototype version of the board. The key elements of this board are the six, 1 mm-diameter, unplated vias between the stubs and the feedline with 0.3 mm above and below the holes. In a future, currently untested version of the tuner based on collaborator Fisher's latest work, the vias would be reduced in size to $350 \mu\text{m}$ to match the width of the updated silicon

chips and diameter of the microlenses being utilized [40]. The two larger holes on either side of the board align with the larger holes on the upper two corners of the control board to allow the vias to be aligned with the laser diodes, as pictured in Figure 5.6. Markings on the board indicate the intended orientation with respect to the PA and antenna in the test bench.

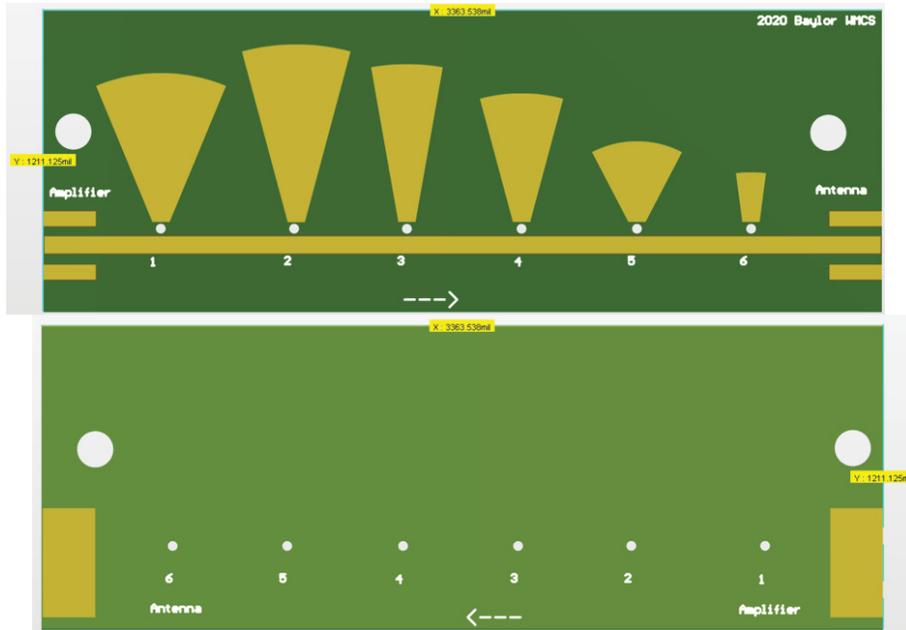


Figure 5.5. RF board. Top layer (top) and bottom layer (bottom)..

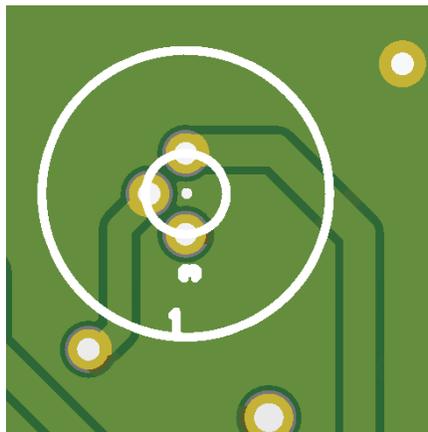


Figure 5.6. Alignment with diode pins (control board) and via (RF board)..

The small white circle, between the three pins and concentric with the two larger white circles, is the one of the six RF board vias, aligned with one of the six laser diodes. In the physical design, nylon screws and standoffs are used to align, connect, and properly space the board apart from each other using the two sets of two larger holes mentioned previously. The constructed control board can be seen in Figure 5.7, RF board in 5.8, and both together in their Poly Cyclohexylenedimethylene Terephthalate glycol-modified (PCTG) housing in Figure 5.9.

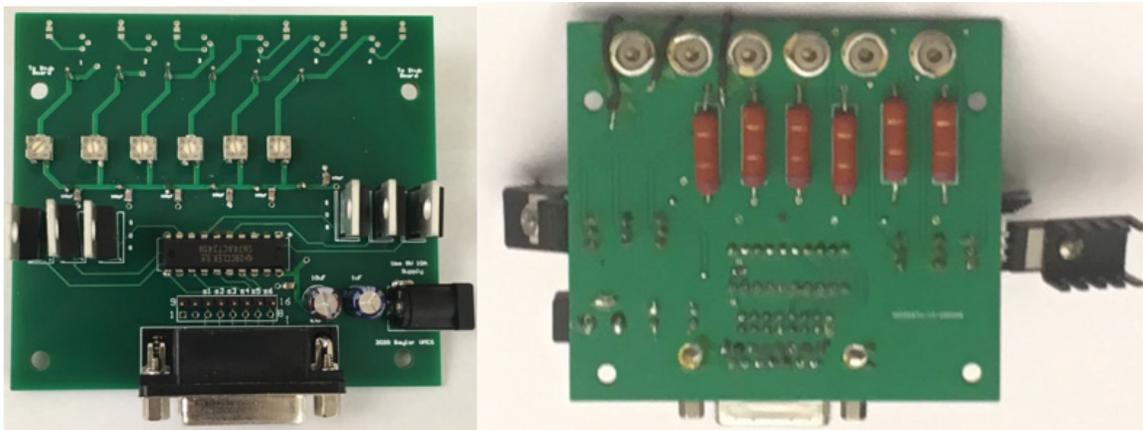


Figure 5.7. Fabricated and assembled control board top (left) and bottom (right).

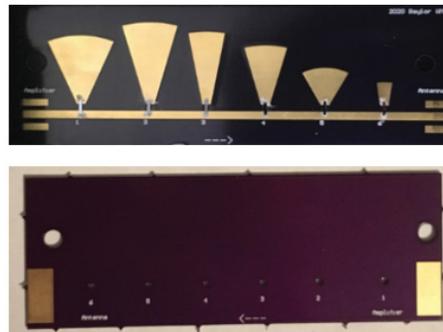


Figure 5.8. RF board top (top) and bottom (bottom) layers.

Notice the longer-than-usual SMA connectors on the RF PCB. These connectors were chosen in order to allow the board to be enclosed in the housing while still being able to connect external RF coaxial cables without holes around the connectors where

stray beams from the diodes could escape. One thing to be noted in Figure 5.10 is the washer towards the base of the SMA connector to block these holes with plenty of connector still available for attaching to equipment.

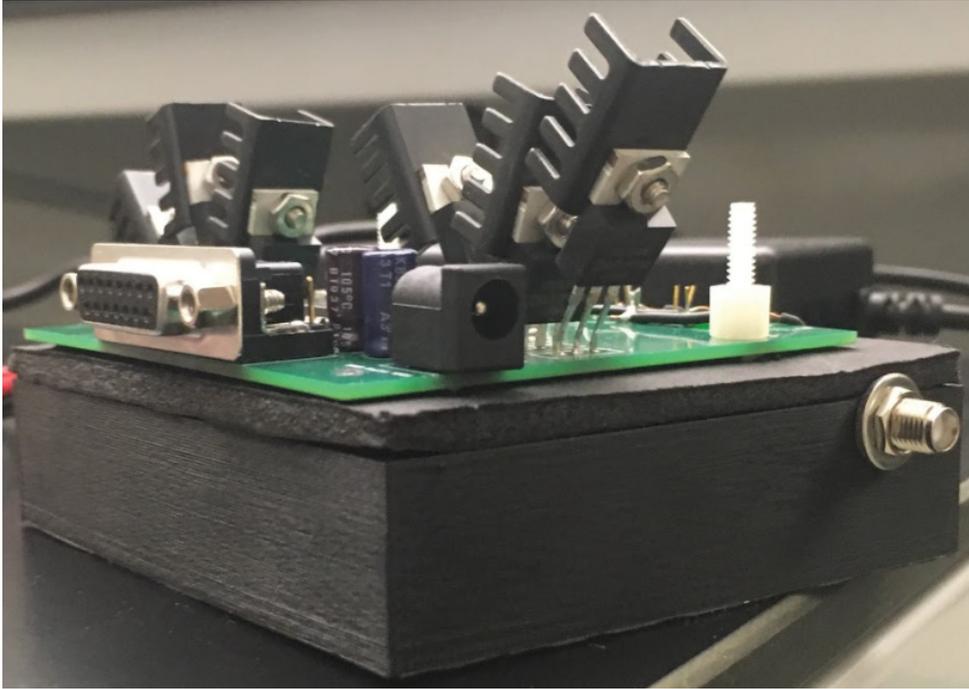


Figure 5.9. Tuner in 3-D printed housing.

Once both boards were fabricated and assembled, the alignment between the vias and diodes were tested visually using a near-infrared (NIR) detector card. When the shape of the laser spot on the NIR card sufficiently met what was expected based on the laser spot size and circular shape of the vias, testing on the tuner began, starting with reflection coefficient characterization.

S-Parameter Characterization of Tuner with Varied Silicon Chipllets

Much like for the low-power prototype, the first set of measurements taken with the new tuner was an S-parameter characterization of the device using a VNA to take the measurements and a microcontroller to communicate with the tuner. Instead of 1001

different frequencies between 2 GHz and 4 GHz, 401 points were used for these characterizations. Multiple versions of chiplets were used with varying semiconductor technology and geometry, but the first chiplets used are the same type as described in [24]. They are 3.175 mm long by 0.5 mm wide with a thickness of 0.2 mm and a gap length of just 0.075 mm; they use a lightly doped silicon material. The results for the characterization using these chiplets is pictured in Figure 5.10. As before, the S_{11} reflection coefficients for all 64 possible tuner states are shown at 2 GHz, 3 GHz, and 4 GHz, from left to right.

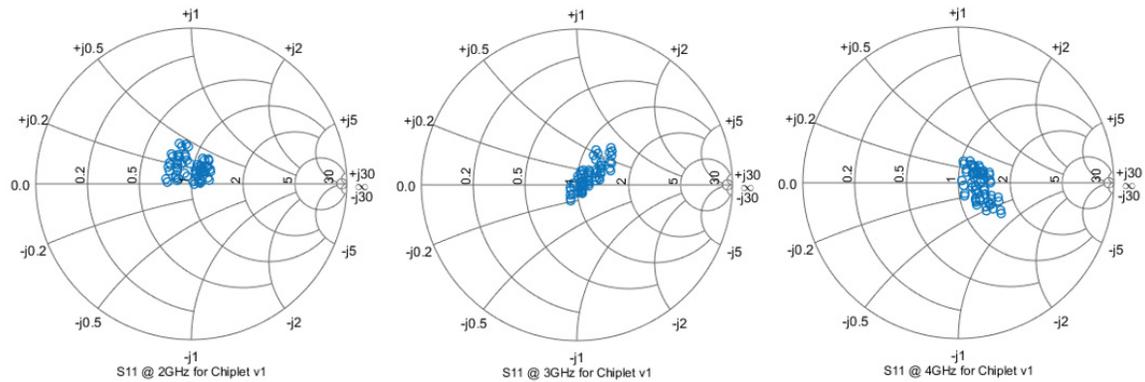


Figure 5.10. S_{11} reflection coefficients from measurement data using original chiplet version at 2 GHz (left), 3 GHz (middle), and 4 GHz (right).

It is immediately noticeable that the reflection coefficient coverage on the Smith Chart is nowhere near as desirable as that of the low-power prototype. It was determined that the available reflection coefficients were drawn near to the center of the Smith Chart by the excess loss of the switches, and the loss was plotted to investigate this issue further. Figure 5.11 shows the loss plotted for all 64 states. (4.4) was used to calculate the loss here as well as everywhere else that loss is mentioned in the thesis. Figure 5.11 can be compared to Figure 4.12 from the low-power prototype. The loss plot confirms the

initial response from seeing the Smith Chart plots; for most tuner states at most frequencies, the loss is much greater than was the case for the low-power prototype. Notice how the traces on the plot remain relatively flat but vary from around 1 dB of loss to around 8 dB. This hierarchy of loss exists due to the large resistance seen when each switch is closed. The lines towards the bottom of the plot have less switches closed than the ones towards the top.

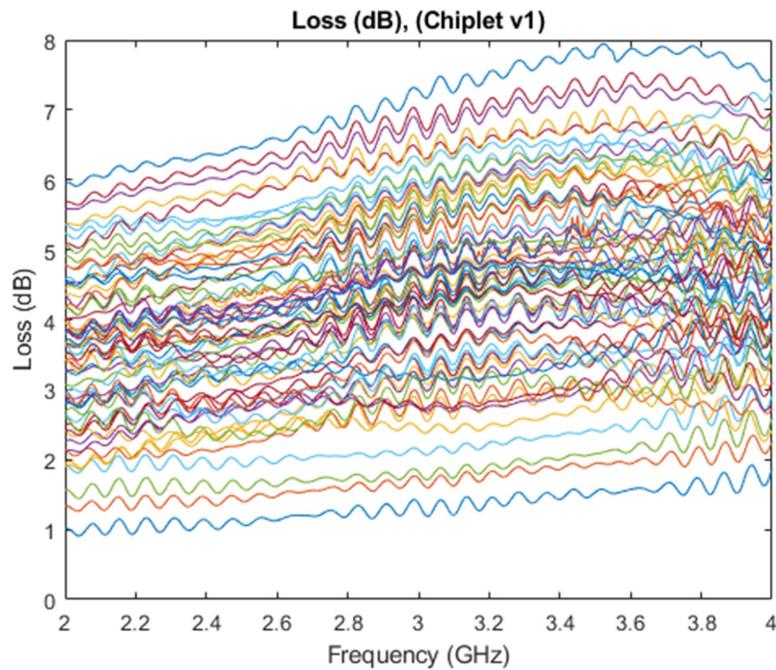


Figure 5.11. Power loss (dB) plotted for all tuner states across octave for first chiplets.

After these results were seen, the next step was to test the same tuner using different types of chiplets prepared by collaborators. Figure 5.12 shows a comparison of the four different types of chiplets used for these measurements. The first version is the type used for the measurements shown in Figures 5.10 and 5.11, and results for the other three will be displayed next. The first version, denoted “v1”, use a lightly doped silicon technology, and the other three versions of chiplets use intrinsic silicon. The length of the

chiplets remains constant at 3.075 mm, but the width, gap size, and taper change, as indicated in the figure. Recall that the vias on the RF board are 1 mm in diameter, so all three new sets of chiplets are wider than the vias, so no light will enter the via and miss the chiplets.

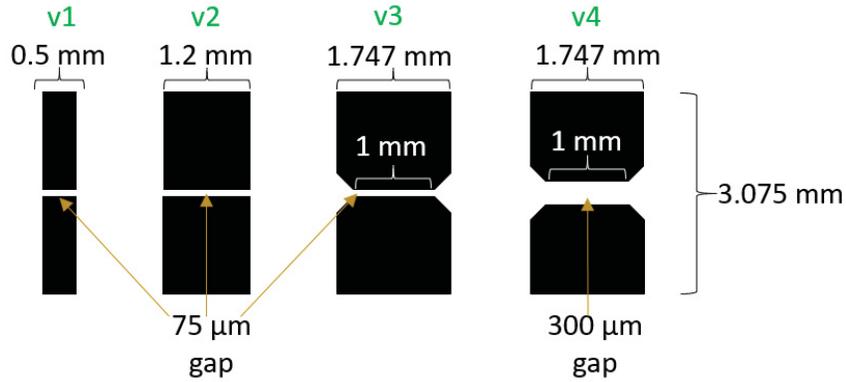


Figure 5.12. Silicon chiplet dimensions.

Figures 5.13 and 5.14 show the reflection coefficients achieved with the second version chiplets and the loss incurred when using them. Figures 5.15 and 5.16 do the same for the version 3 chiplets and likewise for Figures 5.17 and 5.18 with the version 4 chiplets.

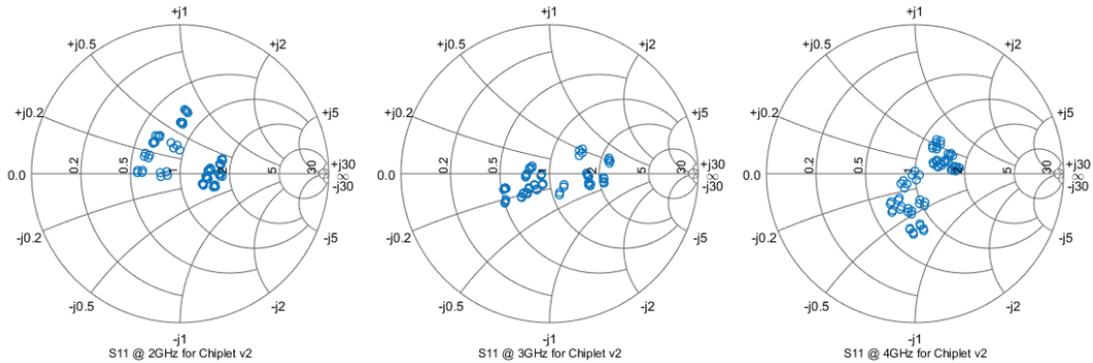


Figure 5.13. S_{11} reflection coefficients from measurement data using second chiplet version at 2 GHz (left), 3 GHz (middle), and 4 GHz (right).

The reflection coefficient coverage is improved from using the first version of the chiplets but still far from the wider coverage achieved with the low-power prototype. The results using the third version of chiplets is not very different.

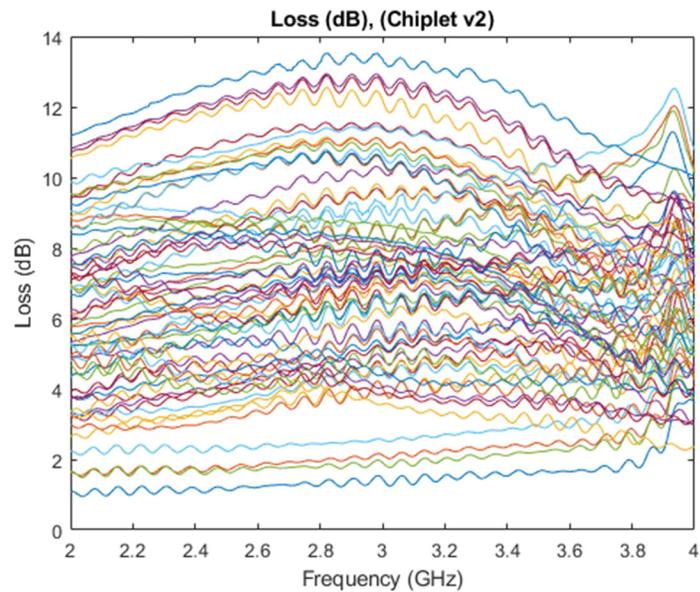


Figure 5.14. Power loss (dB) plotted for all tuner states across octave for second chiplets.

The loss is not very much improved over the first version of chiplets either. Some of the states do have similar loss values near 4 GHz.

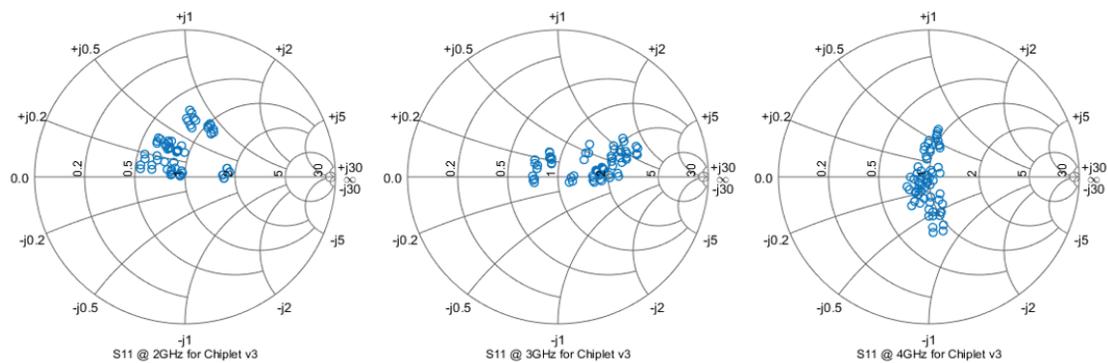


Figure 5.15. S_{11} reflection coefficients from measurement data using third chiplet version at 2 GHz (left), 3 GHz (middle), and 4 GHz (right).

As mentioned, the third version of chiplets resulted in similar values, so the tapering and wider width of the chiplets had negligible effect on the coverage.

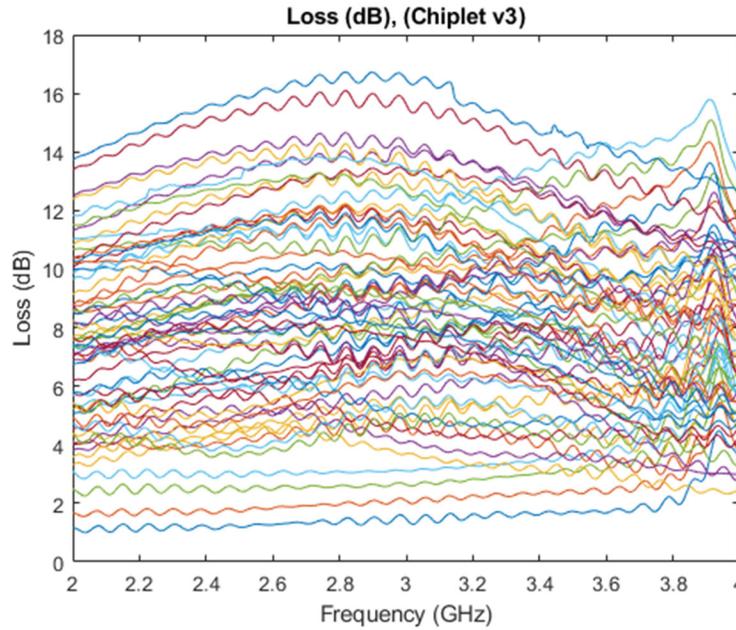


Figure 5.16. Power loss (dB) plotted for all tuner states across octave for third chiplets.

The amounts of loss achieved are similar, with the third version of chiplets incurring slightly more, but the general shape of Smith Chart plots vary only in minor ways with no significant rotations or spreading.

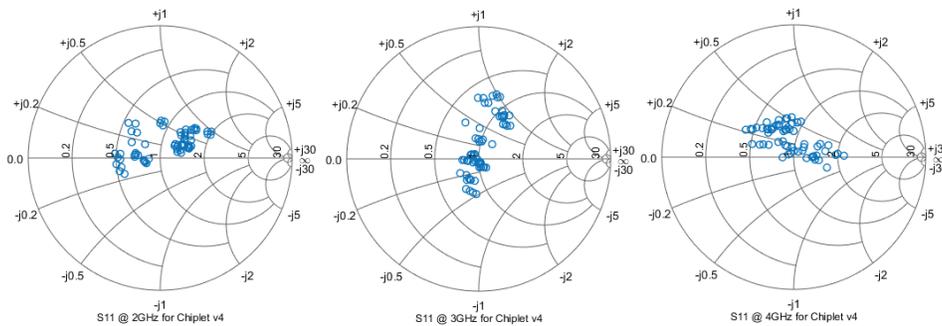


Figure 5.17. S_{11} reflection coefficients from measurement data using fourth chiplet version at 2 GHz (left), 3 GHz (middle), and 4 GHz (right).

The S_{11} plots for the fourth version of the chiplets is also similar to the second and third versions, perhaps marginally more spread out. There is a definite rotation of the points around the Smith Chart, likely due to a change in capacitance with the wider chiplet gap.

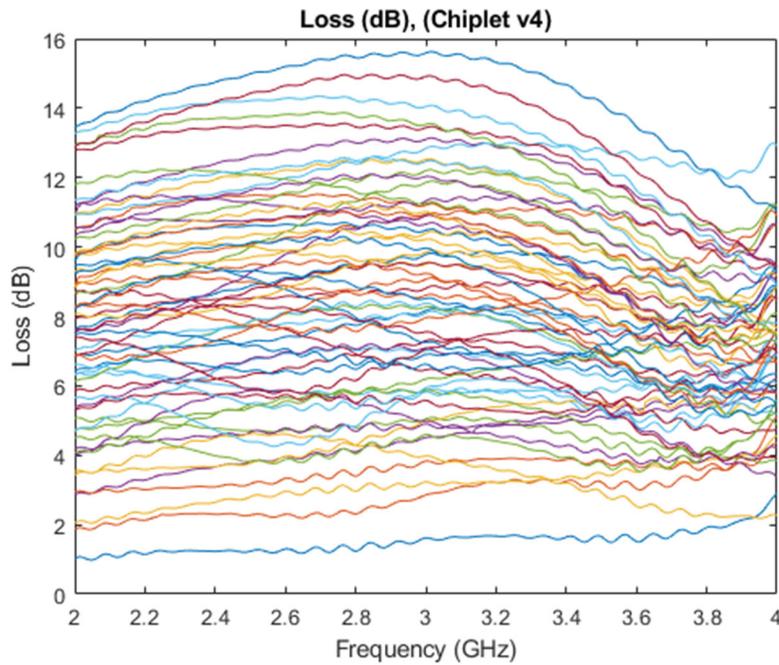


Figure 5.18. Power loss (dB) plotted for all tuner states across octave for fourth chiplets.

Like the previous chiplets, the loss performance was also poor for the fourth version. The blue line seen at the bottom of the chart, representing the lowest loss for nearly every frequency in the octave, is the state with zero switches closed.

The results from the different versions of the chiplets did not meet the performance goals, but the data provides some useful information. Chiplet geometry is unable to solve the problem of power density incident upon the chiplet gaps. At this point, the lenses introduced earlier in Chapter Five were integrated into the design. To

remain consistent with the current design, lenses with a diameter of 1 mm were used, as this was the size of the vias on the RF boards. These lenses also had an antireflective coating, and the 808 nm wavelength of the laser diodes was included in their operating range. Gradient index (GRIN) rod lenses and spherical ball lenses were considered, and the GRIN lenses were chosen due to slightly better loss performance and their added ease of assembly. Collaborators performed initial testing of each type of lens and offered this recommendation. One spherical lens was kept in the board as it was already held in place and very difficult to remove. The lenses were placed in the vias against the chiplets, glued in place, and the tuner boards were reconnected as usual with precautions taken to not flex the RF board too greatly which could force lens through a chiplet. Figure 5.19 shows an image of the two boards together with three of the lenses and laser diodes visible.

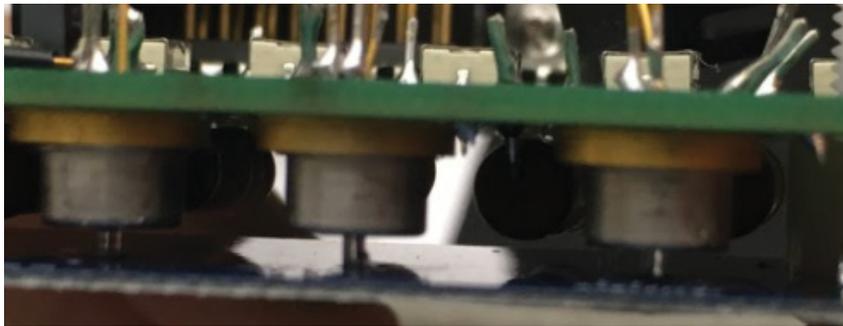


Figure 5.19. Up close view of three laser diodes against three GRIN microlenses.

Because the vias were concentric with the laser diodes, the lenses were as well. Once alignment was checked once more with the NIR detector card, the same measurements were performed with the tuner with the lenses included. When the RF board with the lenses was constructed, another new set of chiplets was used. The fifth version chiplets were 350 μm wide, still 3.075 mm in length, and had a 75 μm gap.

Intrinsic silicon was used. Figures 5.20 and 5.21 show the Smith Chart plots with reflection coefficients and the loss plot, just like for the other four versions of the tuner. There are a handful of clumps of redundant points near 2 GHz, but across the band, the Smith Chart coverage is much improved from the previous four versions of the laser diode/silicon chiplet tuner, near the performance of the low-power prototype and potentially better at high frequencies. The loss results were not as encouraging, but the tuner with lenses still outperformed any of the iterations without them present in the search algorithm testing.

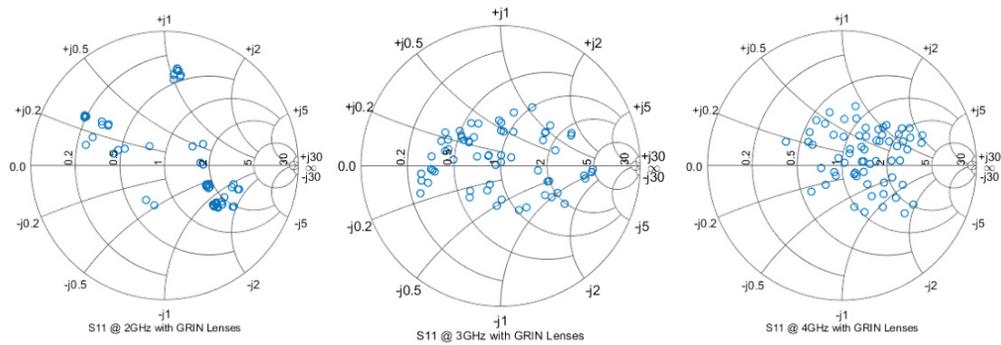


Figure 5.20. S_{11} reflection coefficients from measurement data using fifth chiplet version and GRIN lenses at 2 GHz (left), 3 GHz (middle), and 4 GHz (right).

This is similar to previous versions, but more pronounced here is that certain states demonstrated better loss performance at low frequencies and other states demonstrated better loss performance at high frequencies. This ended up being a critical feature during algorithm testing.

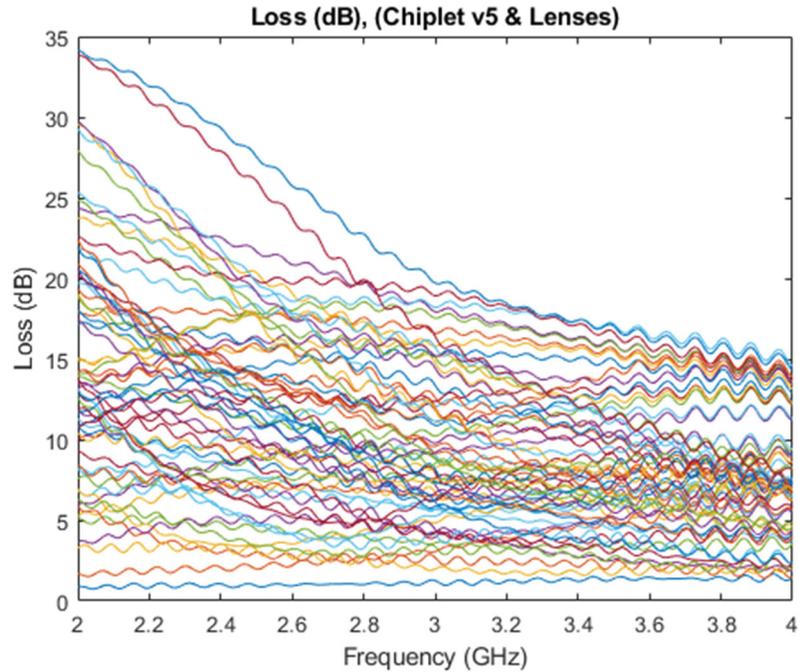


Figure 5.21. Power loss (dB) plotted for all tuner states across octave for lenses and fifth version chiplets.

Besides S-parameter characterizations of various versions of the tuner, the time necessary for the switches to open and close was also tested. Unlike the low-power FET switches, the timing was unknown and varied based on chiplet type.

Measured RF Open and Close Time of Switches with Varied Silicon Chiplets

The opening and closing time of the switches is crucial, as speed of algorithm convergence is a top priority. In order to measure the on and off time of the switches, an RF oscilloscope was used, capable of 20 gigasamples per second, meaning that it could perform measurements at the required time resolution of the open and close time of the switches, unlike a VNA which was attempted first. Figure 5.22 shows the test setup used for measuring the open and close time.

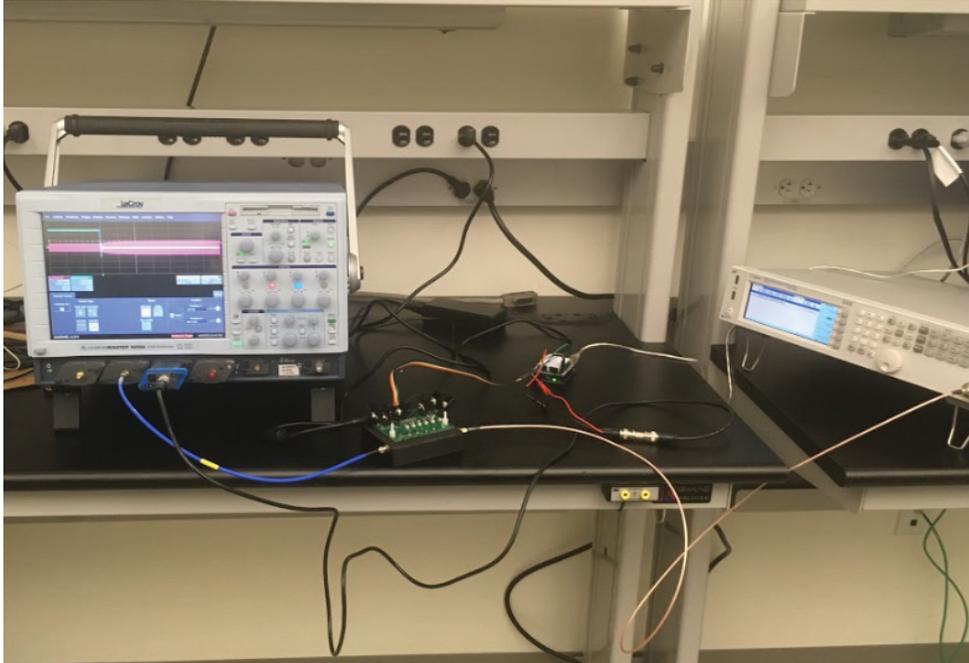


Figure 5.22. Timing measurement test setup.

On the right is an RF signal generator which was used to generate a 3.3 GHz, 0 dBm tone. In the middle of the two pieces of test equipment are the tuner and the microcontroller. The microcontroller was used to turn the laser diodes on or off. On the left is the RF oscilloscope, set to trigger on either the rising edge or falling edge of the microcontroller signal depending on whether the switches were being opened or closed. One channel of the oscilloscope was used to measure the RF signal at the output of the tuner, and the other channel used a high-impedance buffer, allowing it to take non-50 Ω measurements and was connected to the microcontroller's control signal. The timing was determined by observing the power level of the RF tone. To make this easier, to measure the switch open time, all switches began closed, resulting in the highest loss state of the tuner. Transitioning to the state with all switches open, the lowest loss state in many scenarios, provided the most defined difference in open and closed power levels. The

experiment was performed in reverse to measure the close time of the switches. The 90/10 metric was used to provide the timings with an analytic. This is the time taken for the RF tone's power level to transition from a change in 10% from its original value to a change in 90% from its original value, a common metric used for switching time. Figures 5.23 and 5.24 will show the on (close) and off (open) timing of the second version of chiplets, and table 5.1 will show the results for the other four version of chiplets, measured in the same manner. The large blue signal is the RF tone where the power level varies upon switching. The orange signal is the microcontroller control signal with the amplitude divided by 20 to put it on the same scale as the RF tone. Other lines are placed to mark the starting power level, final power level, 10% rise/fall from the starting power level, and 90% rise of fall from the starting power level. The times from the x-axis values at the 10% mark and 90% mark are subtracted from each other to determine the 90/10 on/off times of the switches.

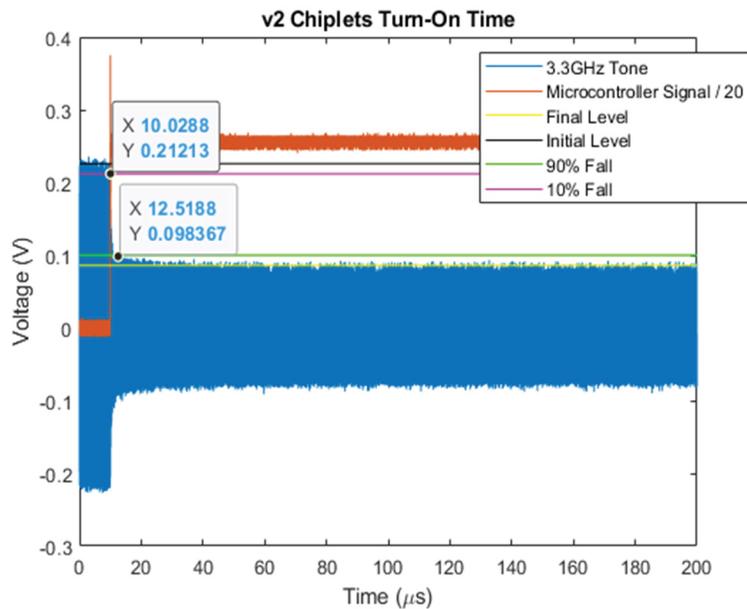


Figure 5.23. Second version chiplet turn-on time with markings.

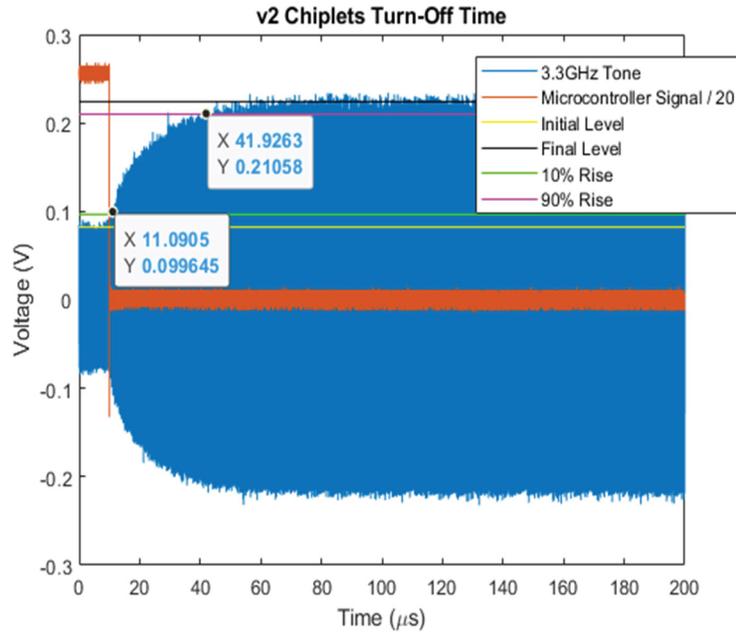


Figure 5.24. Second version chiplet turn-off time with markings.

From those plots, the on time was calculated to be 2.49 μs , and the off time was calculated to be 30.83 μs . Each of the chiplets which used intrinsic silicon experienced similar results with the off time being an order of magnitude higher than the on time. This timing is related to the carrier regeneration rate in the material, and for intrinsic material, the number of free holes and free electrons is equal. In doped materials, there are more free electrons, so the regeneration rate increases, because there are more electrons to fill the same number of holes.

Table 5.1. Switch timing for varied chiplets. v5 chiplets had lenses.

v1 Chiplet On (v1 Chiplet Off)	v2 Chiplet On (v2 Chiplet Off)	v3 Chiplet On (v3 Chiplet Off)	v4 Chiplet On (v4 Chiplet Off)	v5 Chiplet On (v5 Chiplet Off)
2.54 μs (4.07 μs)	2.49 μs (30.83 μs)	4.49 μs (37.07 μs)	8.3 μs (50.43 μs)	2.33 μs 21.86 μs

Among the different types of intrinsic silicon chiplets, the timing does still vary with geometry, perhaps due to a higher associated resistor-capacitor (RC) time constant. The microcontroller also sent on and off signals as fast as possible to measure the response of cascaded switching. The result can be seen in Figure 5.25.

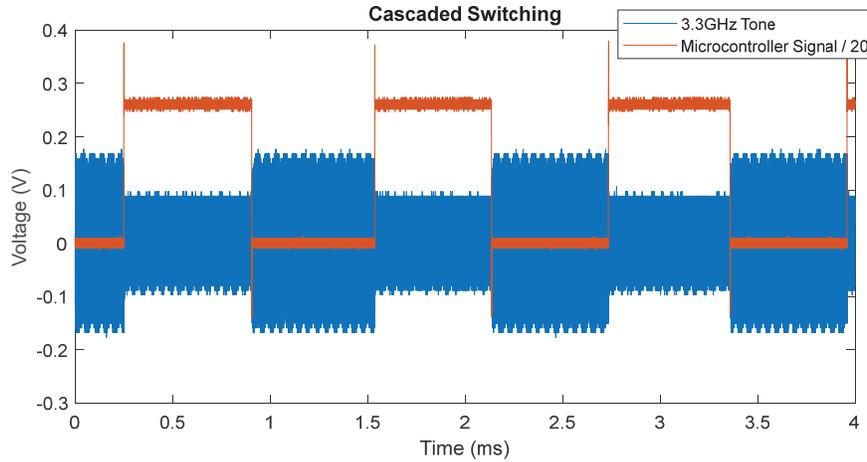


Figure 5.25. Cascaded switching test.

Figure 5.25 shows that the switches responded well to cascaded opening and closing, showing no signs of different behavior. Regardless of chiplet type, these switches limit the algorithm speed compared to the 20-30 ns switching time of the low-power FET switches.

Combined Power Amplifier and Antenna Matching Optimization Results

Most of the groundwork for algorithm testing was performed on the low-power prototype, allowing the tests for the newer version of the tuner to jump straight to searches on the SDR with both the PA and “antenna” tuner in the loop. The only meaningful change made to the algorithm aside from behind-the-scenes details was that the time between measurements was increased from 20 cycles, 5 ns in duration each, to a

higher number, 800 to 4000 cycles, equating to 4 μ s to 20 μ s to compensate for the longer switching times. The measurement setup can be seen in Figure 5.26. It is almost identical to the test bench used in Figure 4.16. For the versions of the tuner before the lenses were integrated, the search algorithm results were poor. Almost any combination of operating frequency and “antenna” reflection coefficient would result in the search converging to state 0 due to the overwhelming loss added by closing a switch, and these results are not shown. Examples of entire tabulated searches have already been shown in Tables 4.4 and 4.5, so Table 5.2 simply shows a summary of the results of five different searches using this tuner. For example, the search on the center row was performed at 3 GHz and an “antenna” reflection coefficient $\Gamma_{ant} = 0.70/-45^\circ$ and completes in just under 200 μ s. The optimum, state 32, corresponding to binary 100000 (switch one closed, remaining switches open) was reached on the second measurement in 23.54 μ s.

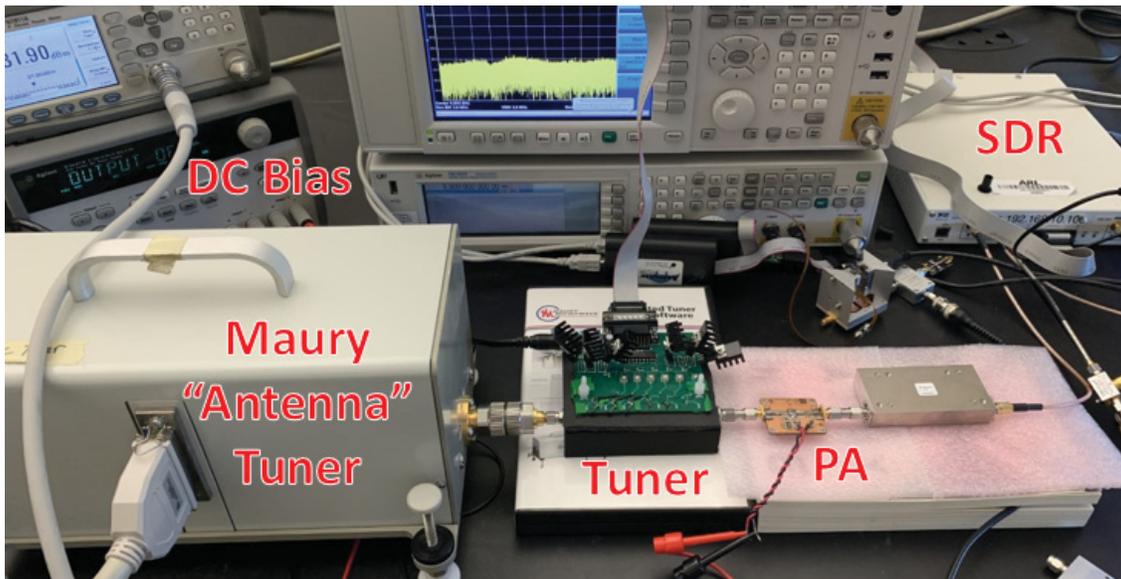


Figure 5.26. Algorithm test bench with laser diode/silicon chiplet tuner.

For these tests, instead of using the MWT-173 FET as the DUT, a Skyworks 65017-70LF InGaP amplifier was used. The SDR was calibrated to provide the PA 3 dBm of input power, regardless of operating frequency. The search described above was performed with 20 μ s built in between measurements, but the algorithm converged to the same optimum in nearly half that time. Depending on the states reached during the search, sometimes the full 20 μ s was required for accurate convergence. These times are an order of magnitude slower than those of the low-power prototype, but still orders of magnitude faster than the state of the art for tuners that can handle high powers.

Table 5.2. Search results for laser diode/silicon chiplet/GRIN lens tuner.

Frequency (GHz)	Γ_{ant}	Number of Measurements	Time (μ s)	Max. Power (dBm)	Best State [Bin (Dec)]
2	0/0°	7	152.44	11.89	000000 (0)
2.5	0.5/45°	12	261.34	8.66	000001 (1)
3	0.70/-45°	9	196.01	11.34	001000 (8)
3.5	0.4/-50°	7	152.44	11.55	100000 (32)
4	0.65/-120°	9	196.01	6.55	001000 (8)

Table 5.2 shows that the search only converged to state zero and states with only one switch closed. Many other searches that converged to the zero state are not shown in the table. The reason that so many searches converged to the zero state is because loss is introduced whenever additional switches are closed. Other states, as shown, are useful for specific scenarios. Figure 5.27 shows the loss across the octave for just the states to which the search converged, again using (4.4) for the loss calculation.

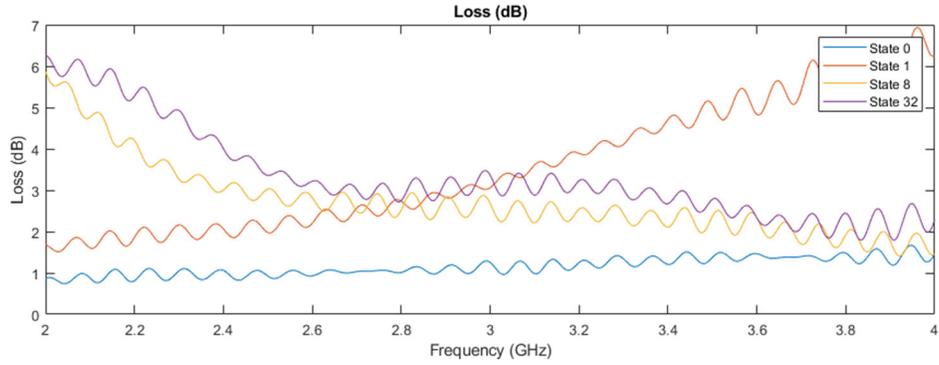


Figure 5.27. Loss for states where algorithm converged.

State zero still appears to be the lowest loss state, but for some scenarios, the other states shown in the Figure 5.27 provide a good enough match to overcome a slightly higher amount of loss which is apparent in the 50Ω scenario. Alternatives such as higher power laser diodes, RF topology changes, and switches in something closer to a single-package device are currently being researched to bring down the loss.

CHAPTER SIX

Conclusions

This thesis has detailed the design of a switched-stub reconfigurable matching network, beginning with simulations and followed by multiple physical prototypes which were used for developing algorithms and further understanding factors which have and will continue to contribute to building even better tuner versions in the future.

The RF topology, utilizing six radial matching stubs, was developed in ADS and used in each iteration of prototypes. The low-power prototype used fast, FET-based RF switches, which provide next to no bottleneck in the reconfiguration process, allowed an algorithm to be developed and entire searches to be performed in under 40 μs [27, 28]. The average search time was improved upon further by integrating starting-point optimization [29]. A higher-power capable version of the tuner was created using custom semiconductor plasma switches which have been shown to be able to handle 35 W [30, 40] of RF power. Various chiplet versions have been incorporated into the design as well as the addition of small focusing lenses in attempts to provide better RF switching performance through the use of more favorable silicon technology and an increase in laser power density reaching the chiplets.

Although the tuner has not yet been tested under high-power RF excitation, plans with collaborators are in place to build identical versions of the tuner using the custom semiconductor plasma switches and integrate one of the two devices into a higher-power test bench in order to investigate its linearity and operation when power levels are closer

to those of an actual device which would be deployed. As the switching technology is improved, new versions will be incorporated into the design as well. As the tuner design continues to improve, the tuner will be tested in a variety of other scenarios, more clearly demonstrating its potential for usefulness in real-life scenarios, much like has been shown by the research group with other tuners in the past [34], taking advantage of the search time which is an improvement of three orders of magnitude. This provides the controlling system additional time-based flexibility and the ability to operate more continuously if the pulse repetition interval is greater than the reconfiguration time of the tuner.

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